JLA420A - DDR5/LPDDR5 Protocol Analyzer

User Manual

JKI
DESIGN for TEST

Version 1.6e

2022-12-21

Contents

1 Version History

Date	Version	Changes
2020-02-11	1.0e	Initial release
2020-04-20	1.1e	Trigger Function is added. Setup GUI is changed
2020-07-28	1.2e	Trigger Setup GUI is changed
2020-09-11	1.3e	Warranty & Calibration service is added.
2021-04-20	1.4e	Update description of Marker.
2021-11-25	1.5e	Update Setup menu for management of json file
2022-12-21	1.6e	Update Setting Guide pin and EyeScan

2 System Overview

2.1 System Configuration

1. JLA420A

2. P4340A

3. PA Streaming Server

4. Probe Cable

5. PCIe Cable

6. PCIe Host Adaptor

7. FireFly Cable Assembly

Module	Description
Hardware	① JLA420A Protocol Analyzer Mainframe ② P4340A Probe Module ③ Storage Server (Option) ④ Probe Cable ⑤ PCIe Host Cable ⑥ PCIe Host Adapter ⑦ Probe Module Cable (*4pcs)
Software	⑧ Instruments Driver ⑨ Protocol Analyzer Software (TeraView2.0)

2.2 Overview

The JKI JLA420A protocol analyzer system is the industry's highest performance DDR5/LPDDR5 protocol analyzer with deep acquisition memory depth up to 512GB and highest sampling rate up to 32GHz. Our high-speed and powerful memory trace solutions enable you to debug and validate DDR based memory systems up to 6.4 Gb/s

Large Memory for Data Capturing

Large memory depth up to 512GB allows you to debug very complex problems by long capturing time.

Ultra-fast Sampling Speed

Ultra-fast sampling speed up to 32 GHz allows you to capture data rate up to 6.4 Gb/s for all channels without any extra options.

Probe Solution

To minimize signal degradation in the probe system, the analog module is separated from the digital module and placed as close as possible to the device.

Interposer Solution

We provide variety of interposer and connecting solutions: LPDDR4/5 interposers, DDR4/5 DIMM interposers

2.3 Features

Maximum Sample Rate

- Max. 32 GHz
- 2/4/8/16/32 GHz options

Number of Channels: total 34 CH

Single-ended channels (31 CH)

- Per-pin termination level
- Per-pin threshold level
- Per-pin timing delay

Differential channels (3 CH)

- 1 Differential clock input (CK)
- 2 Differential strobe input (DQS)

Analysis mode

- Timing mode
- Eye mode

Acquisition Memory

- Max. 512 GB (standard 128 GB)
- Full memory depth up to 32 GHz
- Hardware data compression / Software data decompression

Hysteresis settings for all channels

Host Interface: PCIe Gen3 x8

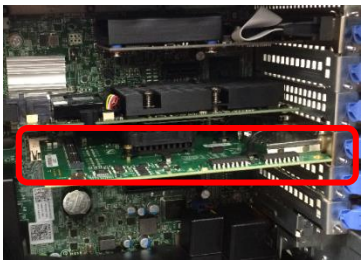
Target application

- DDR4/5 protocol analysis
- LPDDR4/5 protocol analysis

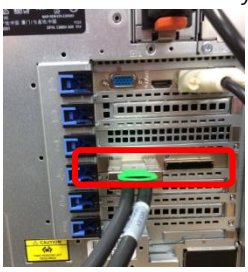
3 Setting Up the Protocol Analyzer

3.1 Installation

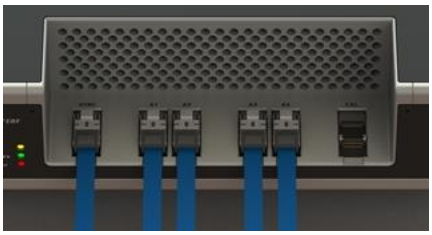
① Install PCIe host adapter card into Host PC's PCIe Gen3 x 16 slot.



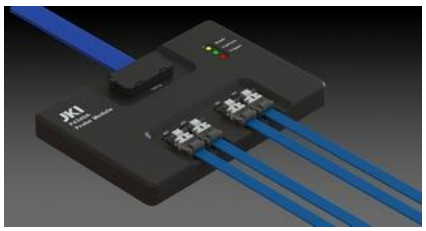
② Connect Protocol analyzer and Host PC with PCIe cable.



③ Connect Probe module cables *4ea between to Protocol Analyzer and Probe Module. (A1:A4 ports) as below.



A1/A2/A3/A4 ←→

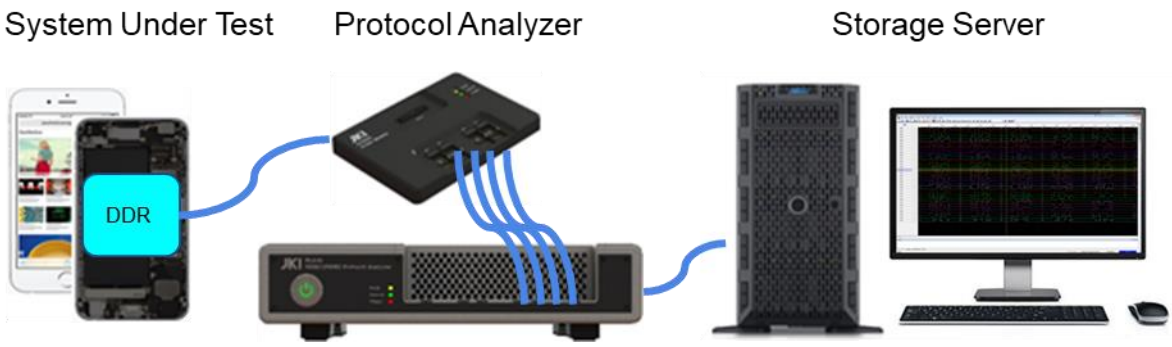


A1/A2/A3/A4 (to same port)

④ Connect Probe module cables* 4ea to Probe Module (A1:A4 ports) .

* Refer to 6.6 Probe Module Cable Assembly Insertion And Removal Instructions.

⑤ Connect the probe cable to Protocol Analyzer and an interposer of Target System



3.2 Turning on Protocol Analyzer

① Power on the Protocol analyzer.

② Power on the Host PC.

③ Make sure the "Ready" (Status LED) is turned on and the "Ready" LED will be lit yellow.
(Check that the yellow LED(Ready) is turned on.)

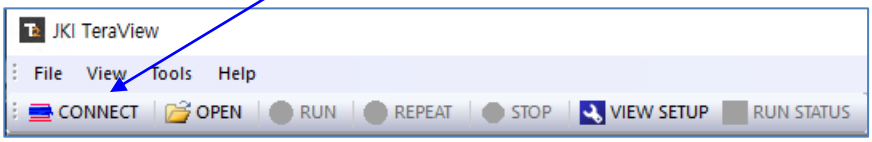
LED	Status	Description
Yellow	Ready	Yellow LED shows that Link is connected to PCIe Gen3 X8 properly.
Green	Capture	During in Capture, Green LED is turned on.
Red	Trigger	Red LED shows that Trigger, which you set, is detected.

3.3 Start Program

On the Windows desktop, double-click the "T2" shortcuts.

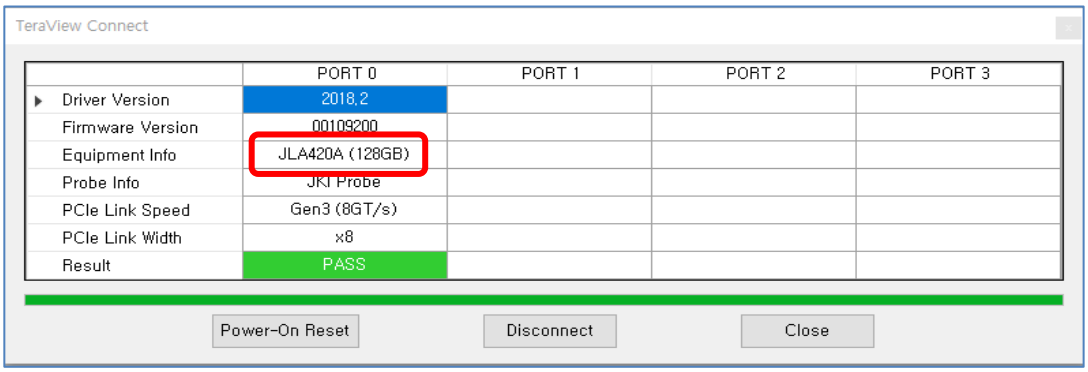
3.4 Connect Instruments

After it runs, click the "CONNECT" in Main menu.

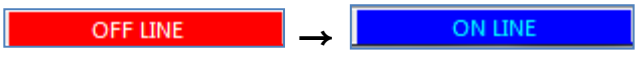


If it is connected successfully, PASS status shows as below.

"Hardware Info." The item displays the size of the memory installed with the name of the connected instrument as shown below.



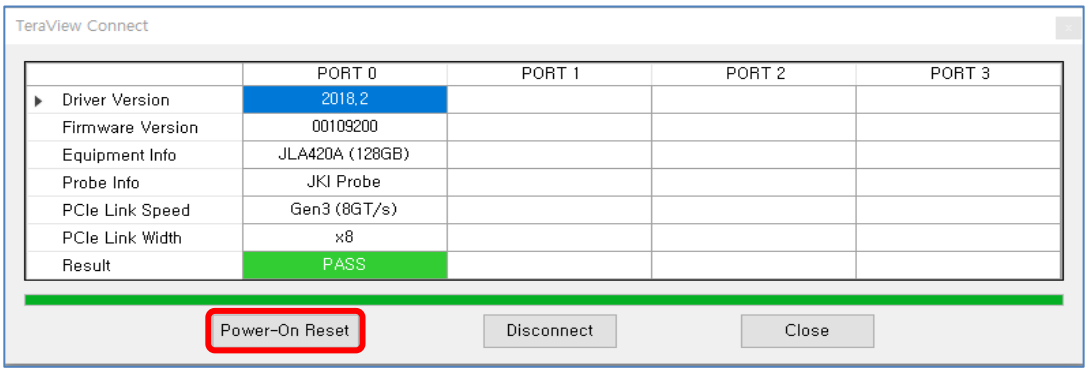
After all the work, Off Line status changes to On Line located at JKI TeraView Screen's lower end as below.



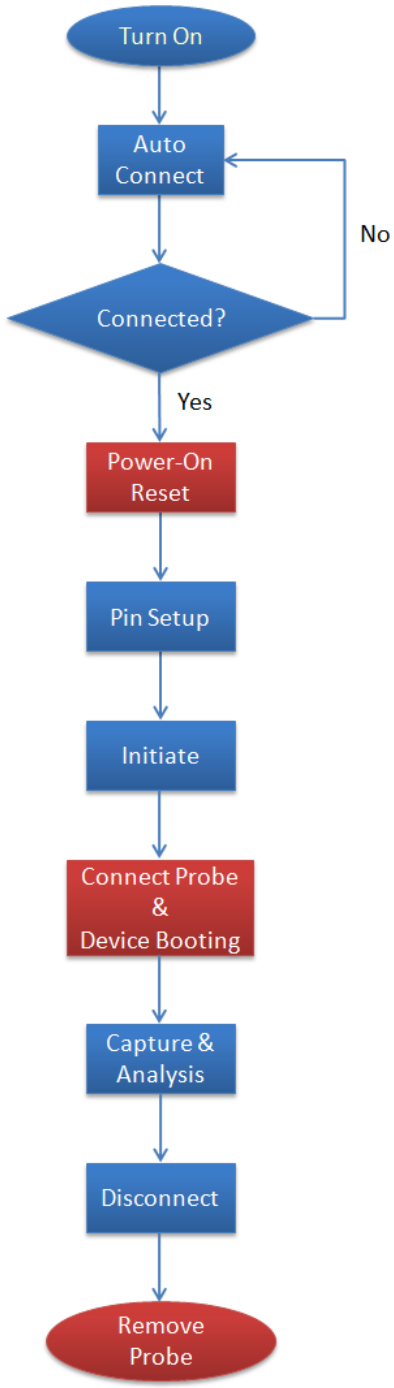
3.5 Power-On Reset

After the equipment power is turned on, the power-on reset process must be performed once.

When disconnecting or turning off the power of equipment, Power-On Reset must be performed.



[TeraView2 Operation Block Diagram]



3.6 Main Window Description

Main Window

- Provide all the menu for equipment control and waveform analysis
- Provide logic timing waveform view and memory protocol list view

Setup Window

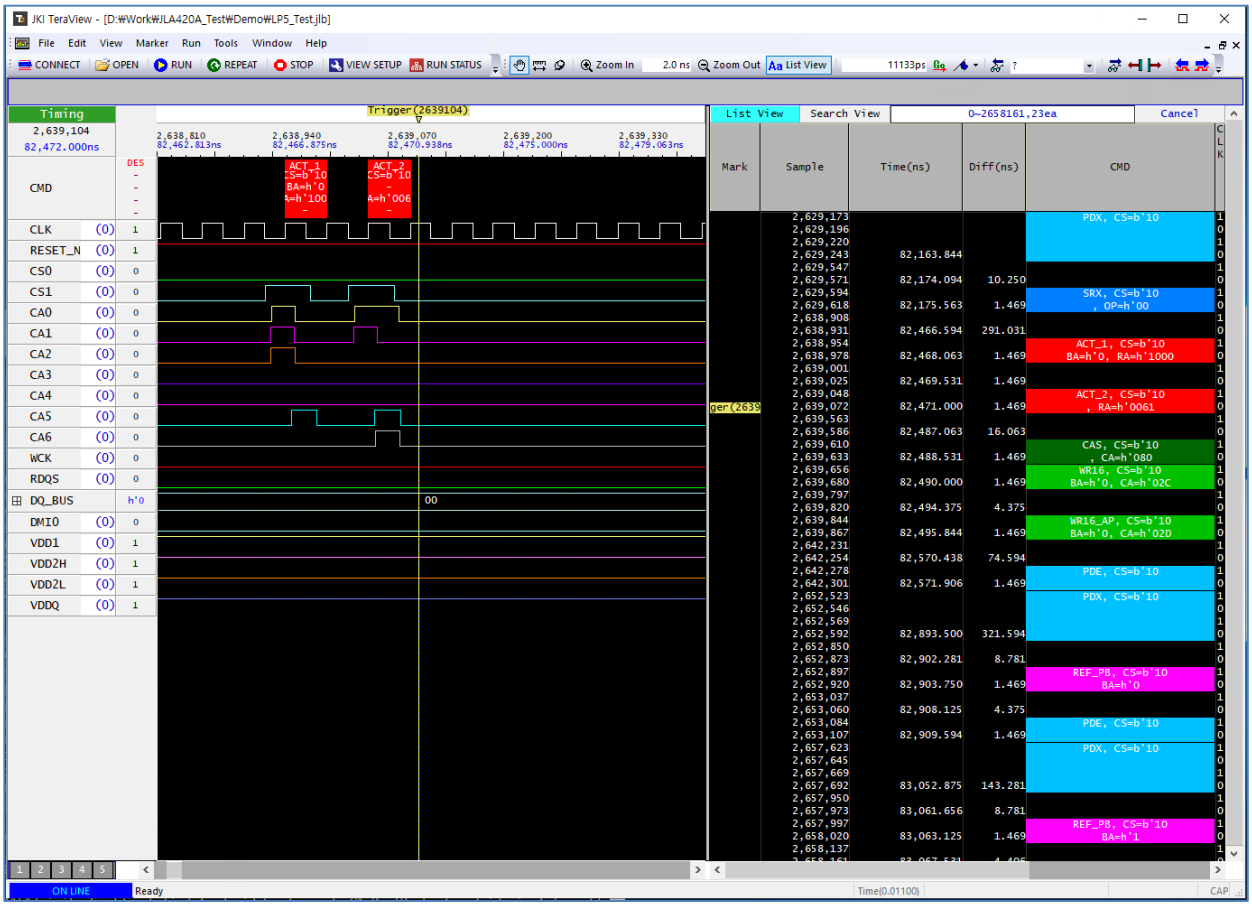
- It is composed of items that set required configuration before starting the measurement
- Set pin information and Trigger condition for each

Run Status

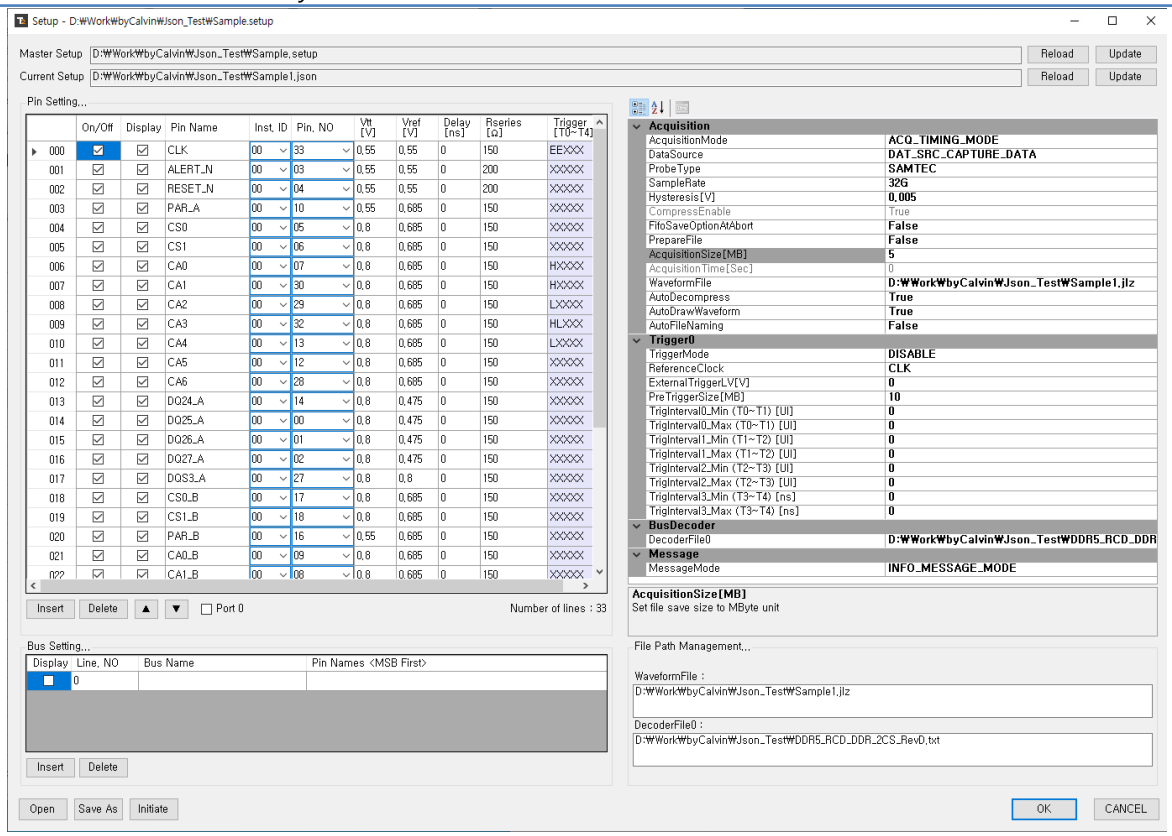
- Show the “Capture” progress after the Run

Eye Window

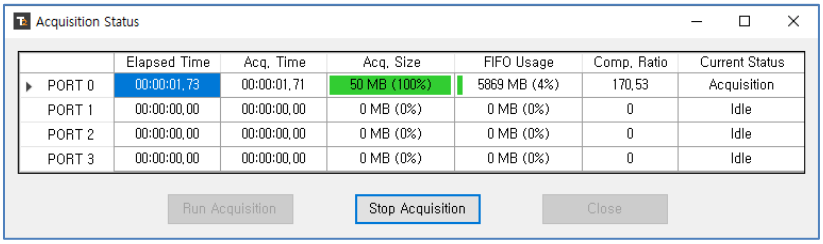
- Run and show Eye diagram



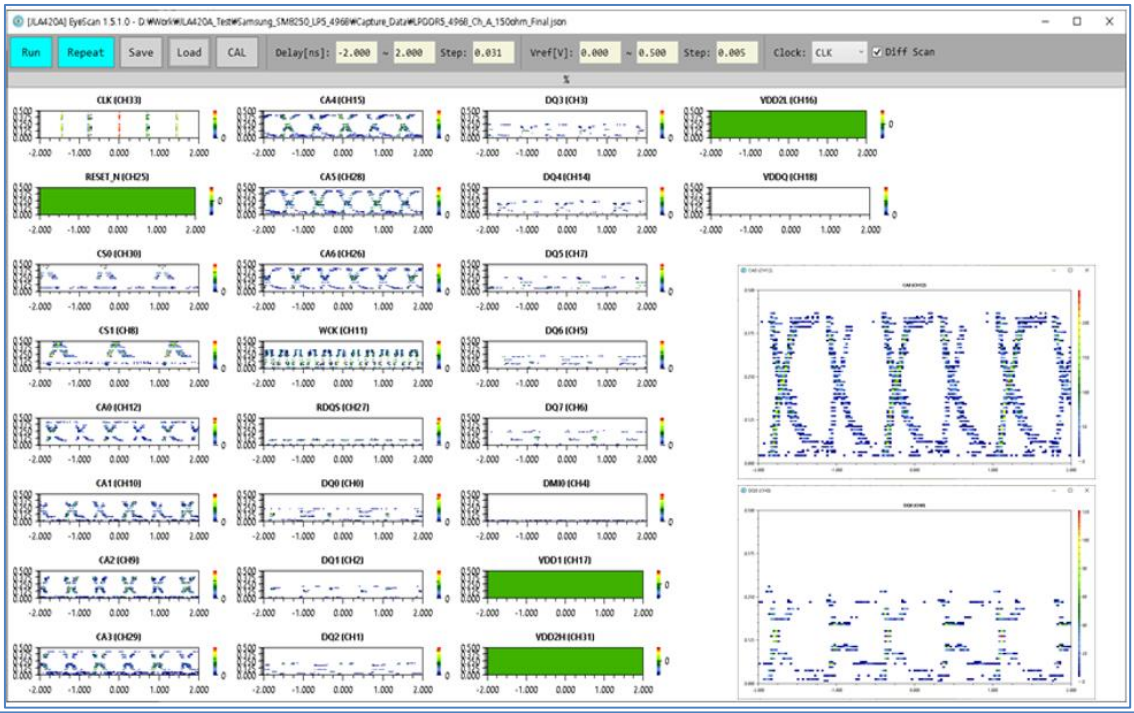
[Main Window]



[Setup Window]

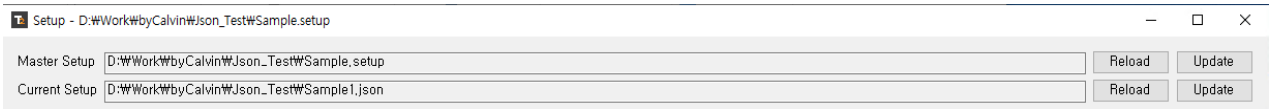


[Run Status]



[Eye Window]

3.7 Management of Setup File



The environment file is divided into the following two types.

- ***.json**

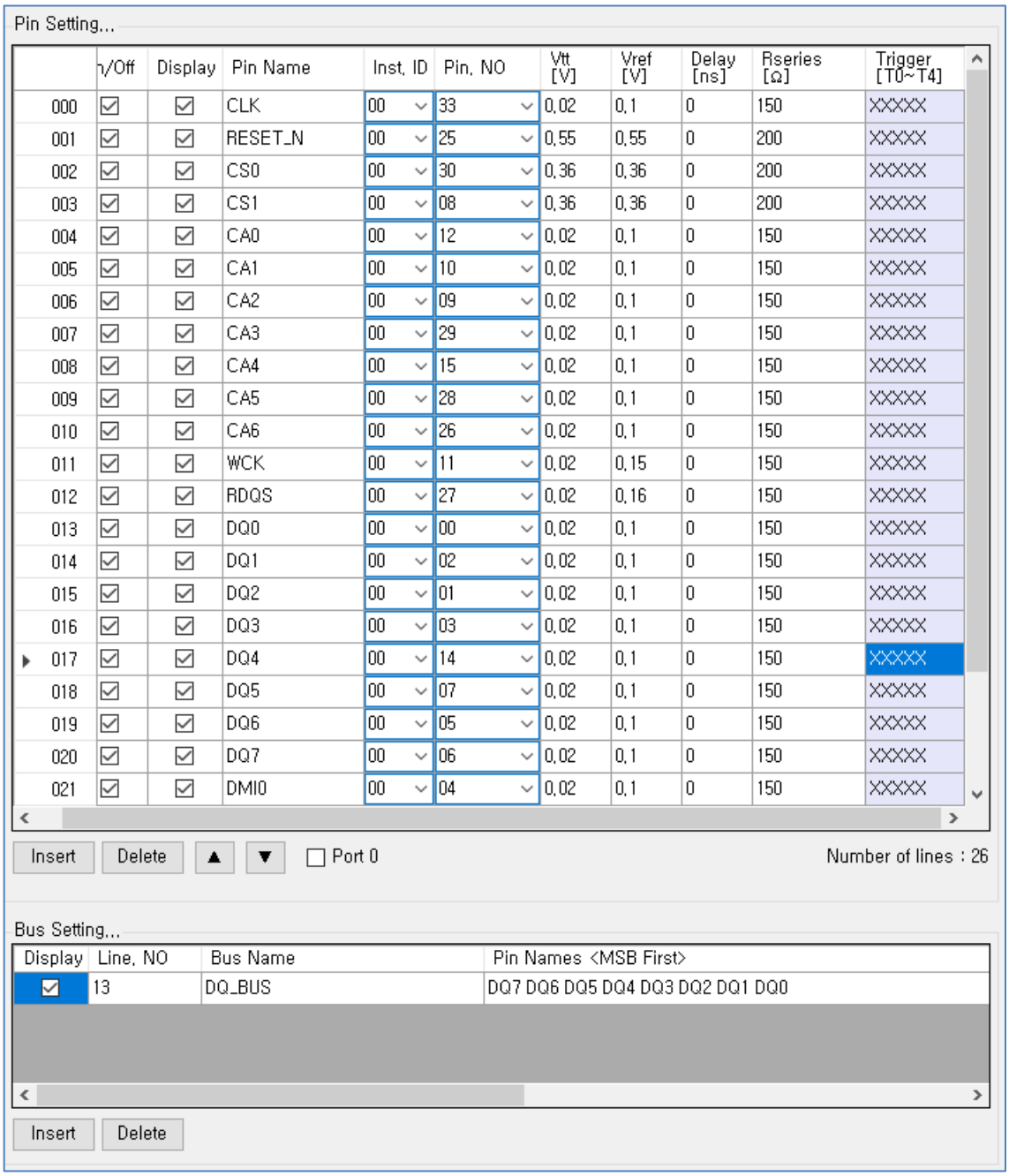
  It is an environment file that is automatically created when a user performs a capture operation.
  The path of this file is automatically created in the location where the waveform file is saved.
  If the user artificially changes the contents of this file (through the setup window), only the following contents are updated. This is to protect the previously captured waveform file (.jlb).

  pin ordering
  bus setting
  Decoder path

  However, when the user performs capture operation with this json file, all modifications are reflected. (When closing the waveform)

Reload : It's used to reload the setting before update.
Update : It's used to update current settings.

3.8 Conditions of Setup Channel



Defining Pin & Bus

Before you can use Protocol Analyzer, you must define buses and pins by

① Adding bus or pin names.

② Select "☐ Port 0" (Port 0 means 1st Protocol Analyzer when you use multiple Protocol Analyzer)

③ Assigning Protocol Analyzer pin to bus or pin names.

④ The following tasks are performed in Pin Setting/Bus Setting (Pin Settings tab):

- Select Insert to add a new pin or bus
- Select Delete to delete a new pin or bus
- Select ▲/▼ to move up/down the order of the selected pin in Pin Setting
- Select Open to open already saved setup file.
- Select Save to save current setup file.
- Select Save As to save a new setup file.

- Select "Initiate" to apply current configuration to this system.
- Port0: Select or except selected port all pins. When It is turned off, Off-pin Data is excluded.
- Pin area: Input each pin's information and Electrical Specification
- Bus area: Show Signals, which tied to the Bus (Classify to MSB first and Space)
- Set All area: An item that separately is inputted from Pin area can be collectively inputted to the all pins
- Pin Name: Determine the name of the pins
- Pin. NO: Select the pin matched to each pin name (refer to Interposer pin-map)

Setting Termination Voltage (Vtt)

- To import signals from the Target System to device, impedance matching is necessary for Signal Integrity. Coaxial cable from JKI equipment is 50 ohm impedance cable. Set to an appropriate value (generally Center value) of the voltage according to the target signal environment. Setting individual or all pins is available
- Range: 0 ~ 1.2V, Resolution: 1mV

Setting Reference Voltage (Vref)

- Set the Reference (Threshold) to determine the measured Voltage High/Low of the signal and Setting individual or all pins is available
- Range: 0 ~ 1.2V, Resolution: 1mV

Setting Timing Delay (Delay)

- To calibrate Timing Skew for each pin, you can set Offset Delay for each pin or all pins is available.
- Range: -2.0 ~ +2.0 ns, Resolution: 31.25ps

Specifying Triggers

- JLA420A(DDR5/LPDDR5 Protocol Analyzer) consists of patterns combination of 34 channels and supports Start capture trigger function.
- You can set trigger for two consecutive Trigger Sequence.
- It consists of 6 pattern types: don't care(X), Low (L), and High (H), Rising edge(R), Falling edge(F), Either edge(E)

X : don't care
L : Low status
H : High status
R : Rising edge status
F : Falling edge status
E : Either edge status

3.9 Pin Condition Setting Guide (basic example : LPDDR5)

Pin Condition setting sequence

- First, set the basic pin conditions (Vtt/Vref) for each pin based on the device datasheet.
- Apply (Initiate) the set Pin conditions to the logic device and check if the Interposer system operates normally.
- If it does not operate normally, move Vtt/Vref up/down appropriately to find the normal operating range.
- If it operates normally, run EyeScan and check the Vih/Vih/Vcm level of each pin.
- Correct Vtt/Vref/Delay conditions for each pin according to EyeScan results.
- Finally, execute capture and check that Command on Bus decoder is measured without Invalid.

Detailed Pin Setting (Reset – CMOS Interface)

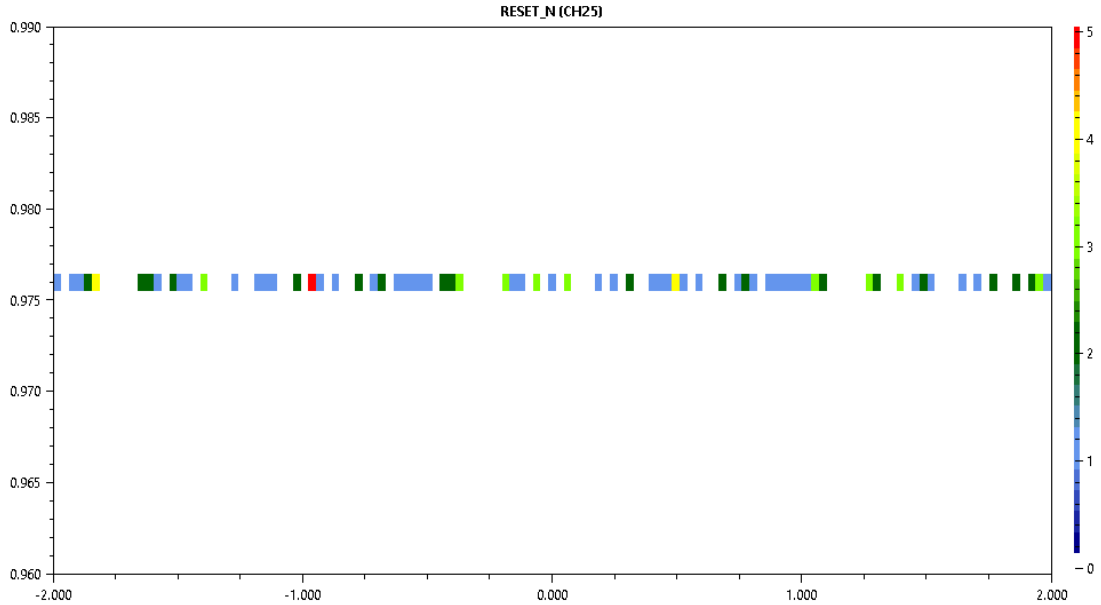
Reference Voltage(VDD2H) : 1.1V

Vtt = Vref = 0.55V

Table 309 — Reset input level specification

Item	Symbol	Min/Max		Unit	Note
Reset_n ViH	ViH_RS	Min	0.8xVDD2H	V	
		Max	VDD2H+0.2	V	1
Reset_n ViL	ViL_RS	Min	-0.2	V	1
		Max	0.2xVDD2H	V	

NOTE 1 Refer LPDDR5 overshoot and undershoot, 12.1.4.



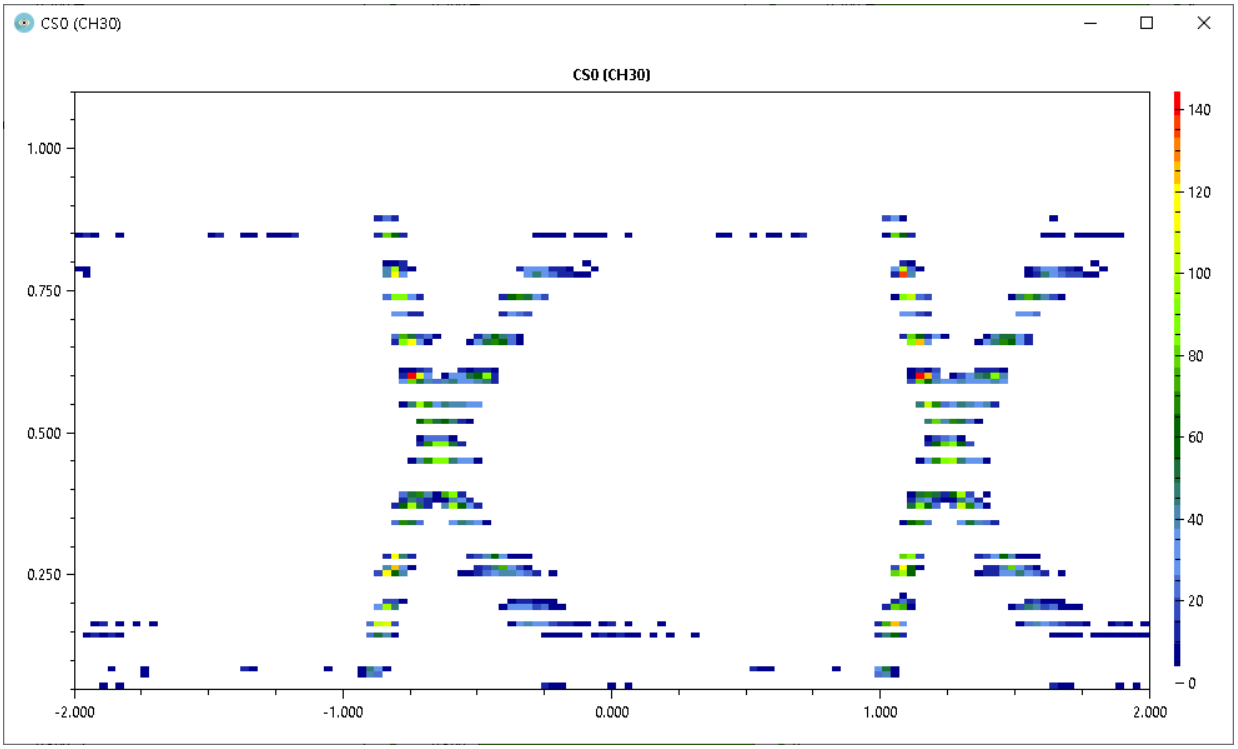
Detailed Pin Setting (CSx – LVSTL Interface)

Reference Voltage(VDD2H) : 1.1V

Vtt = Vref = 0.36V

Table 353 — CS Rx Specification

Item	Symbol	Min/ Max	CK Frequency (MHz)												Unit	Note
			67	133	200	267	344	400	467	533	600	688	750	800		
Rx Mask																
CS Rx mask width at VrefCS	tCSIVW1	Min	0.3												UI	1
CS Rx mask width at vCSIVW	tCSIVW2	Min	0.22												UI	1
CS Rx mask height	vCSIVW	Min	180												mV	2
Rx Single pulse																
CS Rx pulse width	tCSIPW	Min	0.6												UI	
CS Rx pulse amplitude	vCSIHL_AC	Min	240												mV	3
CS reference voltage	Vref_CS		VDD2H/3												mV	
Power down																
CS VIL during Power down / Deep Sleep	ViLPD	Max	130												mV	4
CS VIH during Power down / Deep Sleep	ViHPD	Min	550												mV	5
		Max	VDD2H + 0.2												V	5



Detailed Pin Setting (CA – LVSTL Interface)

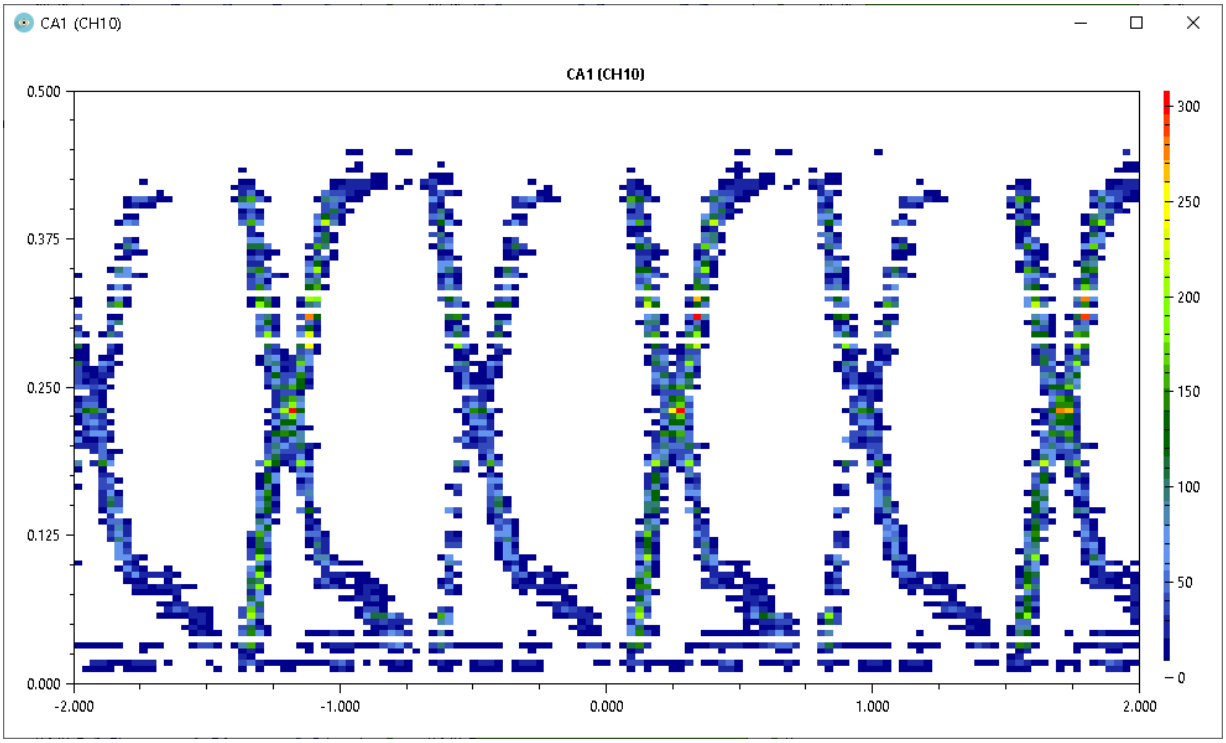
Reference Voltage(VDDQ) : 0.5V or 0.3V

Vtt = Vref = 0.15V (considering ODT condition)

Table 354 — CA Rx Specification

Item	Symbol	Min/ Max	CK Frequency (MHz)												Unit	Note
			67[A]	133	200	266	344	400	467	533	600	688	750	800		
Rx Mask																
CA Rx mask width at TBD	tCIVW1	Min	0.3												UI	1,2
CA Rx mask width at vCIVW	tCIVW2	Min	0.18												UI	1,2
CA Rx mask height	vCIVW	Min	155												mV	3
Rx Single pulse																
CA Rx pulse width	tCIPW	Min	0.6												UI	4
CA Rx pulse amplitude	vCIHL_AC	Min	190												mV	5
CA Vref																
CA Vref	VrefCA	Max	367												mV	
		Min	75												mV	
CA mask offset																
CA to CA offset	tCA2CA	Max	100												ps	6

A) The Rx voltage and absolute timing requirements apply for all CA operating frequencies at or below 67 for all speed bins. For example tCIVW1 (ns) = 4.77ns at or below 67MHz CK frequencies.



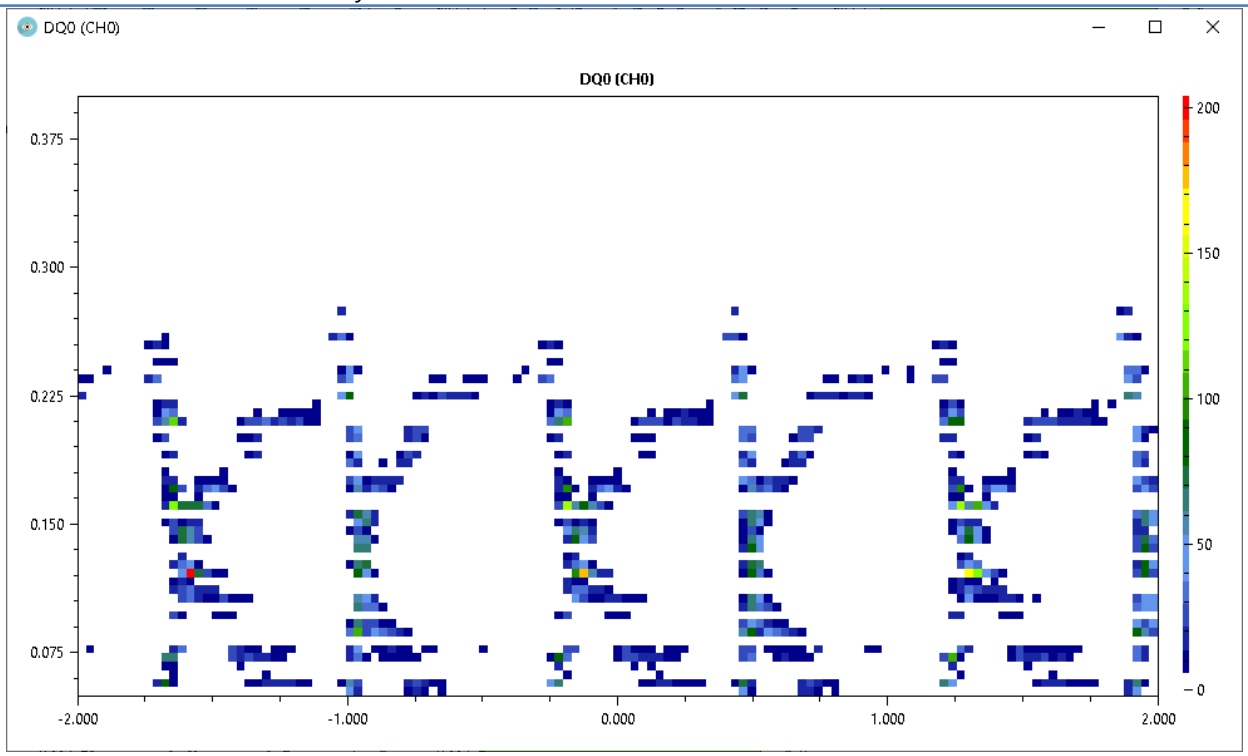
Detailed Pin Setting (DQ – LVSTL Interface)

Reference Voltage(VDDQ) : 0.5V or 0.3V

Vtt = Vref = 0.15V (considering ODT condition)

Table 355 — DQ, DMI, Parity and DBI Rx Specification

item	Symbol	Min/ Max	WCK Frequency (MHz)											Unit	Note
			266	533	800	1067	1375	1600	1867	2134	2400	2750	3000	3200	
Rx Mask															
DQ Rx mask width at TBD	tDIVW1	Min	0.35												UI	1
DQ Rx mask width at vDIVW	tDIVW2	Min	0.18												UI	1
DQ Rx mask height	vDIVW	Min	140			120				100					mV	1,2
Rx Single pulse																
DQ Rx pulse width	tDIPW	Min	0.45												UI	4
DQ Rx pulse width above/below vDIVW	tDIHL	Min	0.25												UI	4
DQ Rx pulse amplitude	vDIHL_ AC	Min	140												mV	3
DQ Vref																
DQ Vref	VrefDQ	Max	350							225					mV	
		Min	75												mV	



Detailed Pin Setting (CK – Differential LVSTL Interface)

Reference Voltage(VDDQ) : 0.5V or 0.3V

Vtt = Vref = 0.15V (considering ODT condition)

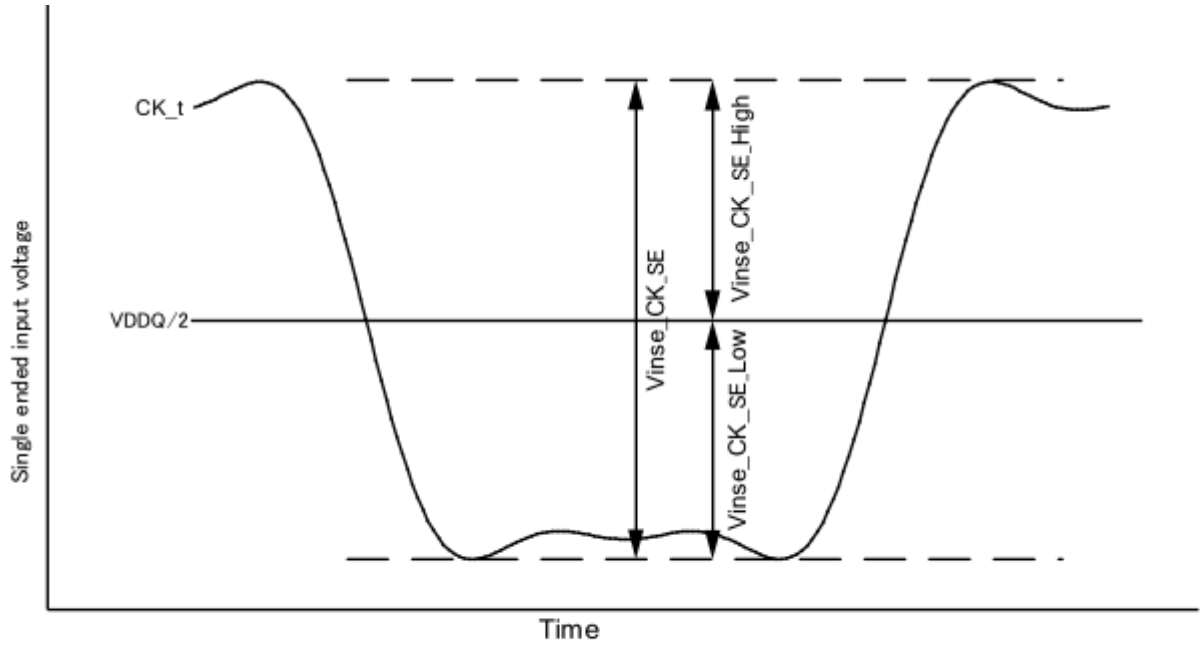
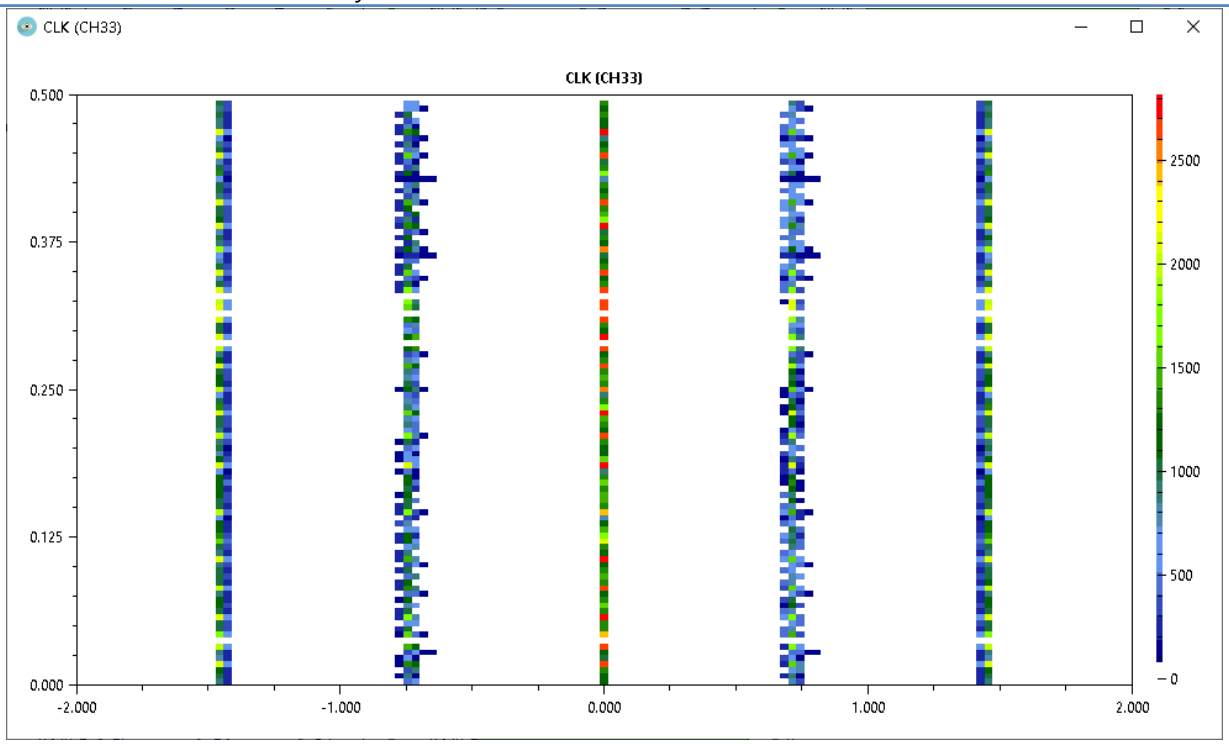


Figure 209 — Single Ended Mode CK input Voltage



Detailed Pin Setting (WCK – Differential LVSTL Interface)

Reference Voltage(VDDQ) : 0.5V or 0.3V

Vtt = Vref = 0.15V (considering ODT condition)

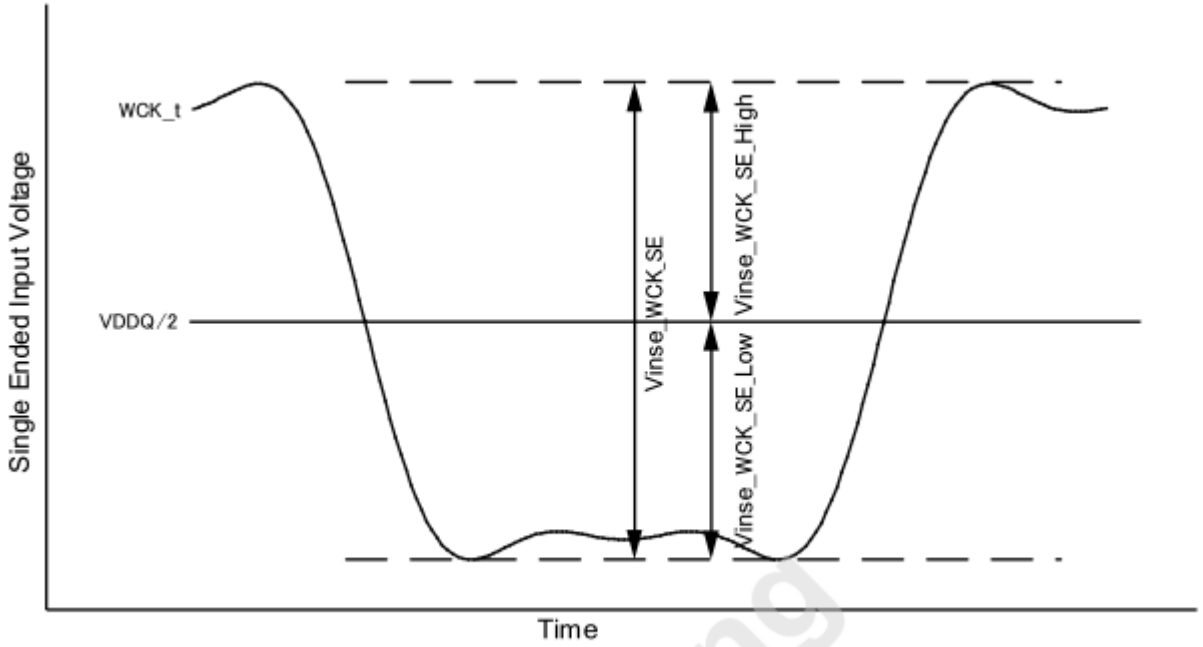
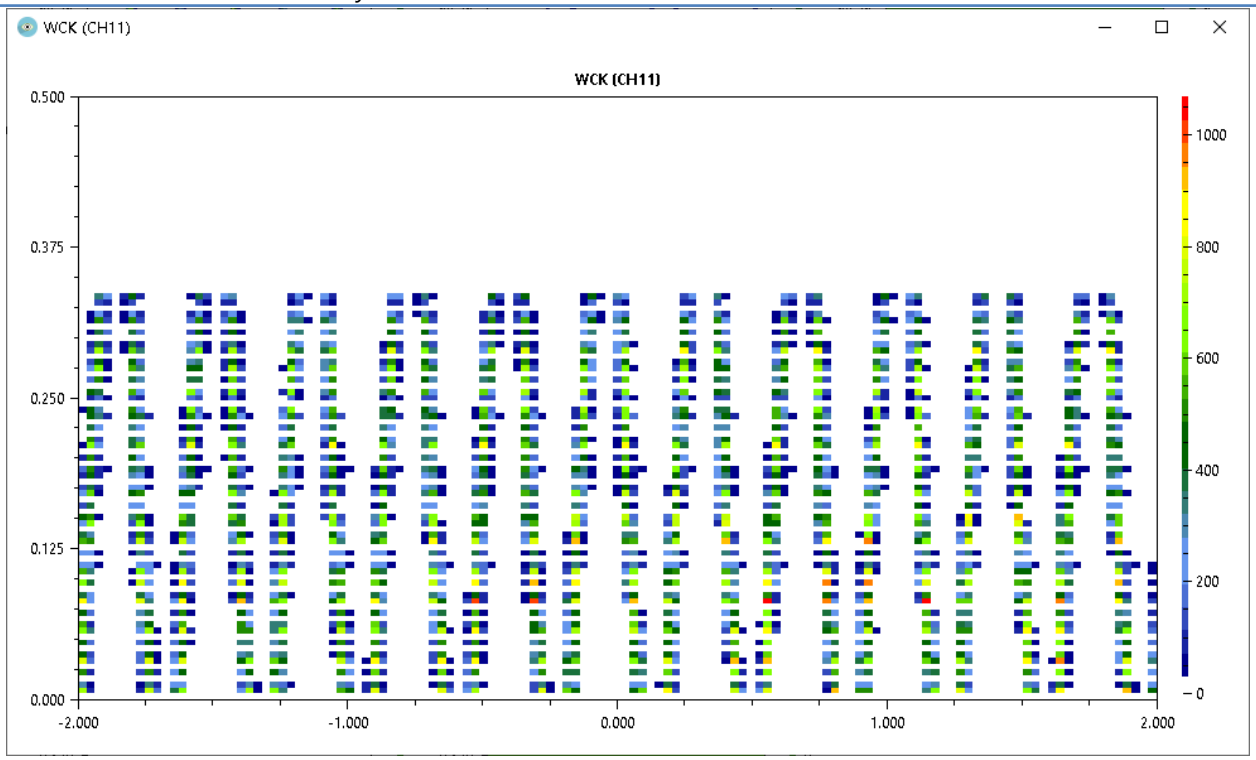
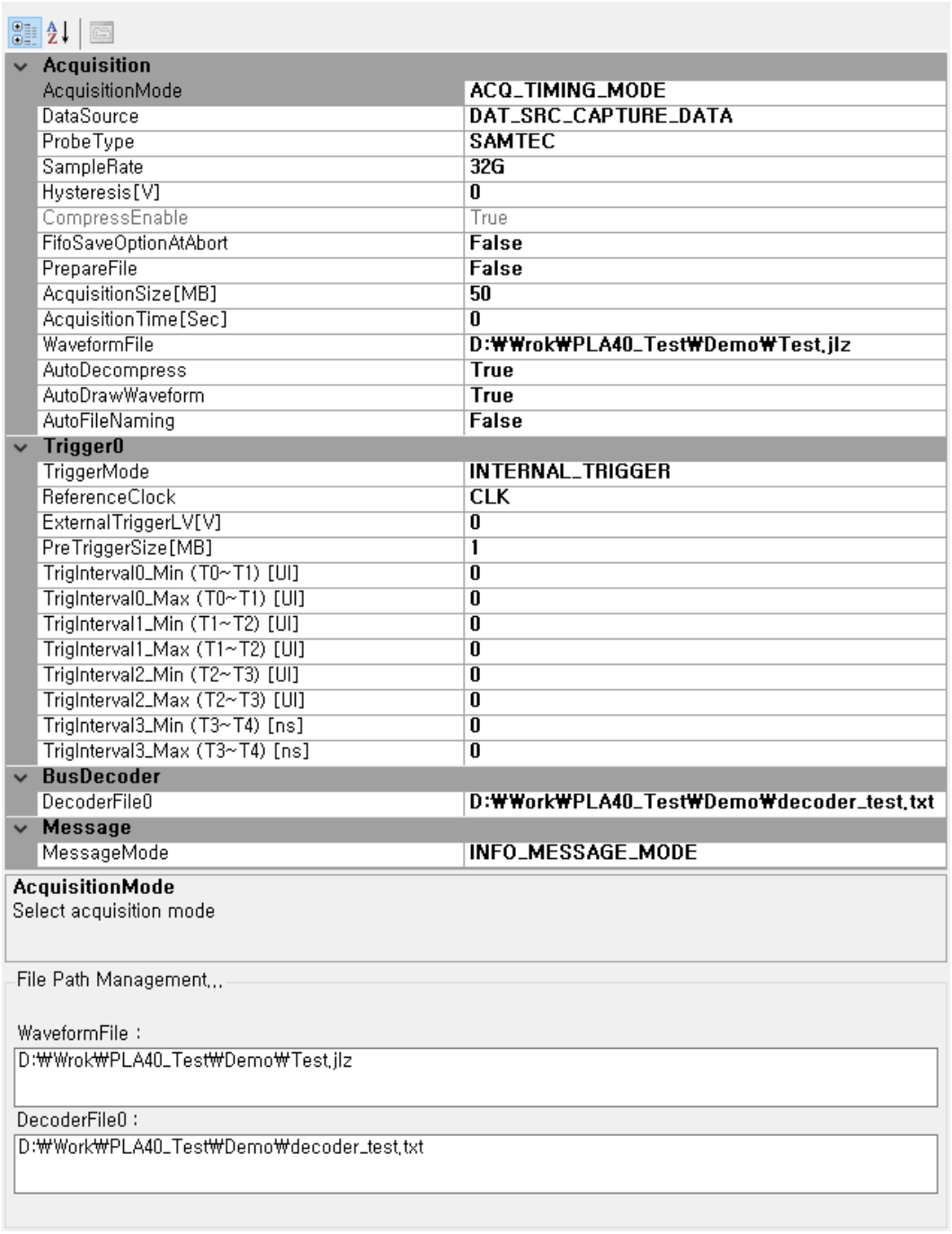


Figure 207 — Single Ended Mode WCK input Voltage


WCK (CH11)
WCK (CH11)
0.500
0.375
0.250
0.125
0.000
-2.000
-1.000
0.000
1.000
2.000
1000
800
600
400
200
0

3.10 Setup Capture Options



Acquisition Mode

Acquisition Mode

- ACQ_TIMING_MODE : This is way of acquisitioning DATA by sampling clock. (Asynchronous mode)

Data Source

- Select “DAT_SRC_CAPTURE_DATA”
  - DAT_SRC_CAPTURE_DATA(default): Acquisition inputted signal from Probe
  - DAT_SRC_LOOPBACK (debugging purpose): For Calibration per each CHs
  - DAT_SRC_COUNTER (debugging purpose): Testing with counter pattern generated internally.

Probe Type

- SAMTEC: SAMTEC Probe connector type
- SOFTTOUCH: SOFT-TOUCH probe connector type

Sample Rate

- Select Sampling rate: 32GHz/ 16GHz/ 8GHz / 4GHz / 2GHz

Hysteresis[V]

- Set hysteresis voltage (Vhys) The difference between the positive-going and the negative-going input threshold voltages.
- Range: 0 ~ 50 mV

Compress Enable

- True: Save the acquisition data with compression (jlz file format)
- False: Save the acquisition data without compression (jlb file format)
- Set always as True in JLA420A

FIFO Save Option at Abort

- When the acquisition stops by the user, it is an option to store the remaining data of FIFO.

Prepare File

- As a function of generating a file in advance to improve performance of file storage, it can improve the Streaming performance acquisition. (requires additional time to generate file before data acquisition)

Acquisition Size

- Input data size for acquisition (unit: MB)

Acquisition Time

- Input time size for acquisition (unit: Second)
- If the acquisition size is satisfied first, the acquisition time is ignored and the acquisition ends.

Waveform File

- Select the file path and name to save the acquisitioned data.

Auto Decompress

- Option to decompress captured data automatically after data acquisition.

Auto Draw Waveform

- An option to display waveform to the screen after data acquisition.

Auto File Naming

- Auto file naming with date and time on acquisition.
- If select true, not overwrite previous acquisitioned file.

Trigger

Trigger Mode

- Select trigger mode for data capture.
- DISABLE: Trigger disable.
- INTERNAL_TRIGGER: Trigger enable to user pattern (T0~T4).
- EXTERNAL_RISING: Trigger enable to external rising-edge signal.
- EXTERNAL_FALLING: Trigger enable to external falling-edge signal.

ReferenceClock

- Select reference edge clock pin name.

ExternalTriggerLV

- Set external trigger voltage level.

Pre Trigger Size

- Select the amount of data capacity to save before Start user trigger condition (unit: MB)

Pre Trigger Time

- Select the amount of time to save before Start user trigger condition (unit: us).

TrigInterval0_Min (T0~T1) [UI]

TrigInterval0_Max (T0~T1) [UI]

- Condition of trigger interval for between T0 to T1.
- TrigInterval0_Min ≤ Interval ≤ TrigInterval0_Max
- Unit : Reference Clock edge

TrigInterval1_Min (T1~T2) [UI]

TrigInterval1_Max (T1~T2) [UI]

- Condition of trigger interval for between T1 to T2.
- TrigInterval1_Min ≤ Interval ≤ TrigInterval1_Max
- Unit : Reference Clock edge

TrigInterval2_Min (T2~T3) [UI]

TrigInterval2_Max (T2~T3) [UI]

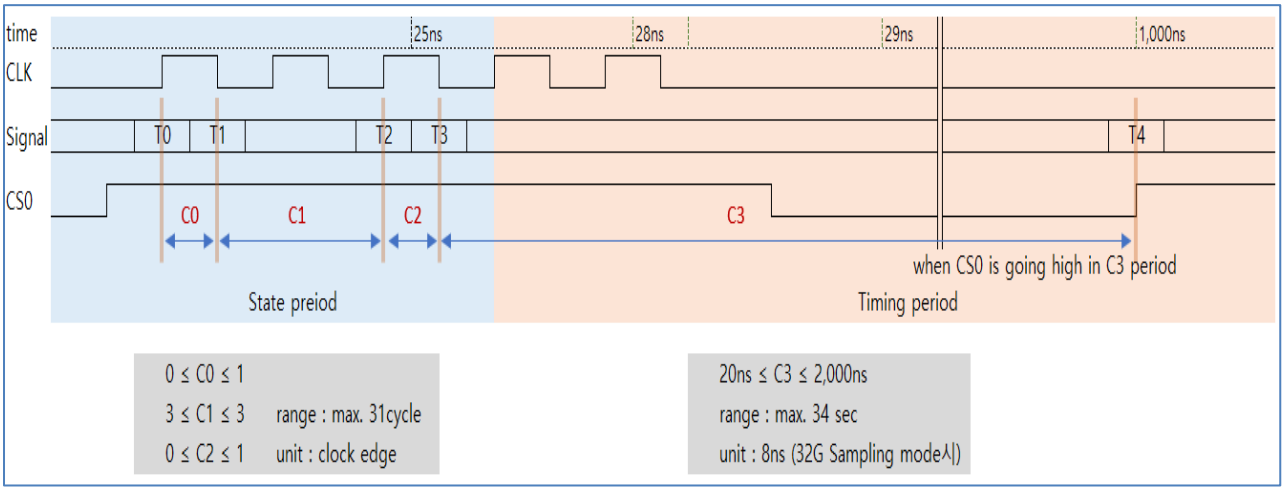
- Condition of trigger interval for between T2 to T3.
- TrigInterval2_Min ≤ Interval ≤ TrigInterval2_Max
- Unit : Reference Clock edge

TrigInterval3_Min (T3~T4) [ns]

TrigInterval3_Max (T3~T4) [ns]

- Condition of trigger interval for between T3 to T4.
- TrigInterval3_Min ≤ Interval ≤ TrigInterval3_Max
- Unit : 16 * SampleRate (ex, 0.5ns at 32G sample rate)

Example Triggering



BusDecoder

DecoderFile

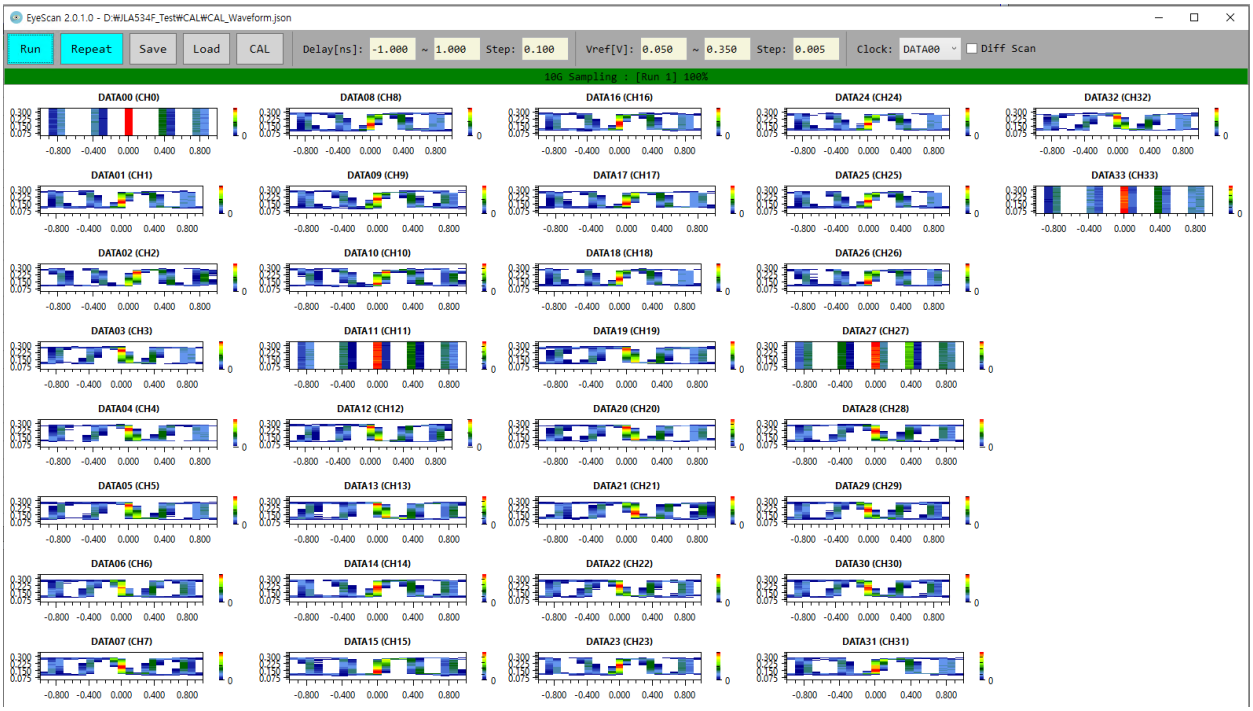
- For command analysis in waveform, select the file in which the condition was stored.

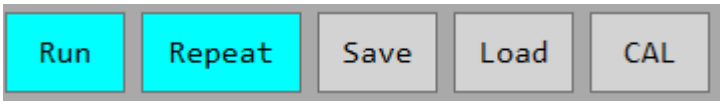
Message

Message Mode

- Set the message output level for debugging.
- INFO_MESSAGE_MODE: Does output to action information level message (default)
- NO_MESSAGE_MODE: Does not output any message

3.11 EyeScan





Run

Capture button for extracting eye diagrams

Depending on the environment settings (Voltage, Time resolution),

if the resolution is high, Capture may take a long time.

Repeat

Button to execute Run repeatedly

In order to extract the Eye Diagram, there must be many toggles of the signals to be measured.

Otherwise, The Eye Diagram is not created normally.

It is a function that allows the user to accumulate and capture for a long time.

When the button is pressed, the button name is changed to Stop.

Capture operation is performed repeatedly until the user presses Stop.

Save

Button to save the captured Eye Diagram

Load

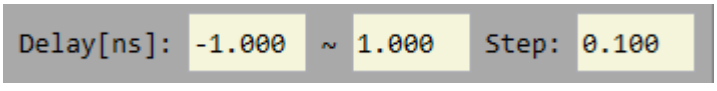
Button to call previously captured Eye Diagram

CAL

A button to calibrate delay and offset voltage for each pin.

A separate Calibration Board is required.

Therefore, this feature is only available to manufacturing suppliers.



X axis Range Setting

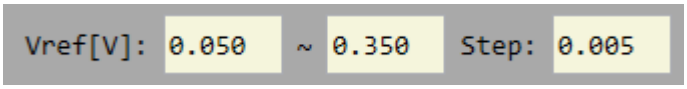
It is set from the '-' direction to the '+' direction based on the 0 point.

If the signal to be measured is 1Gbps, 1UI is 1ns.

Therefore, if you want to see at least 4UI, you can set it to -2.000ns ~ 2.000ns.

X axis Resolution Setting (Step)

It should match the sampling speed of the equipment. In case of 32G sampling, it is about 31.25ps (1000/32) and in case of 16G sampling, it is designated as 62.5ps (1000/16).



Y axis Range Setting

A method of adjusting the reference voltage of the comparator located at the probe stage

Range: 0V ~ 11.99V

Specify the minimum and maximum levels of the swing range of the signal to be measured.

Y axis Resolution Setting (Step)

Minimum step : 0.001V

When this value is small, the resolution is high, but it takes a lot of time to complete scanning.

Therefore, when measuring at first, measure by increasing the value (more than 20mV), and then measure by lowering it if there is no problem in measurement.

For Eye Scanning, a standard clock is required.

In the case of DRAM, since a standard clock pin exists, the pin is designated.

In the case of NAND, DQS is usually designated and used to see the eye diagram of the DQ stage.

If DQS is the standard,

The Eye diagram is difficult to come out clearly because the sources are different when reading and writing.

Therefore, scan must be performed while operating NAND so that Read/Write does not mix.

'Diff Scan' is a setting for Differential Signal,

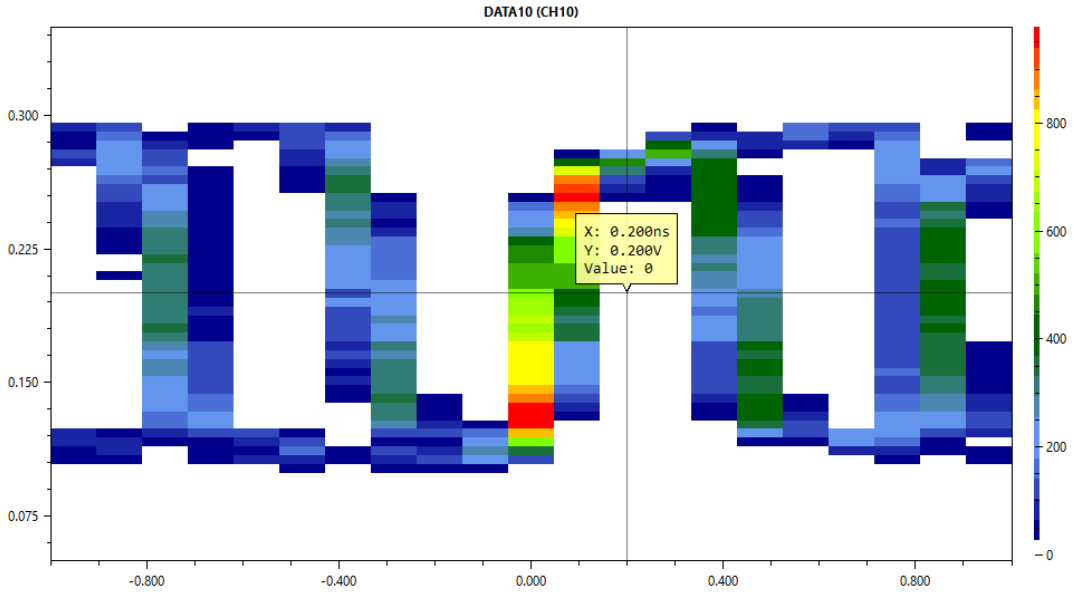
Depending on the connection status of pins 11, 27, and 33, which are fixed differential channels in the equipment, whether or not to check is determined.

If the user connects the probe as a differential, do not check the checkbox.

Check this checkbox if you want to see eye diagrams of No. 11, No. 27, and No. 33 when connected to differential channels with single ended.

Detail Description of Eye Diagram

If you want to see the Eye Diagram in detail on the EyeScan window, double-click the applicable Eye Diagram, and it will be displayed as a large-sized image as shown below.



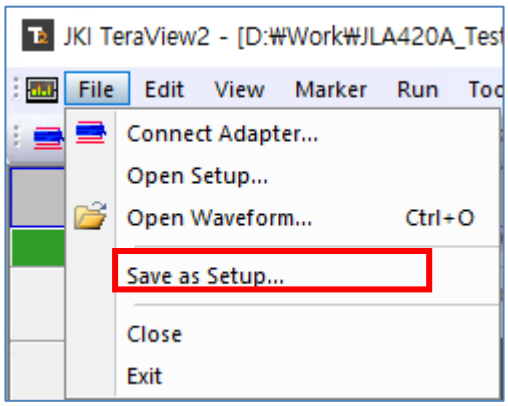
If you press the left button of the mouse, the X-axis and Y-axis values of that point are displayed.
If the left button of the mouse is not pressed, the display automatically disappears.

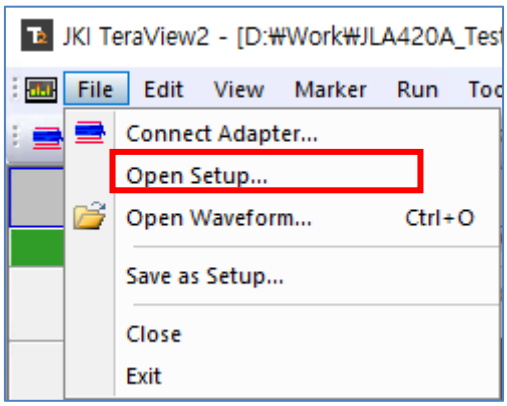
The center level of the measured Eye Diagram is the Vref value. If set to this value, more accurate capture is possible. This is because there is a slight difference from the calculated value due to the hardware characteristics.

3.12 Saving & Loading Configuration

Save as Setup

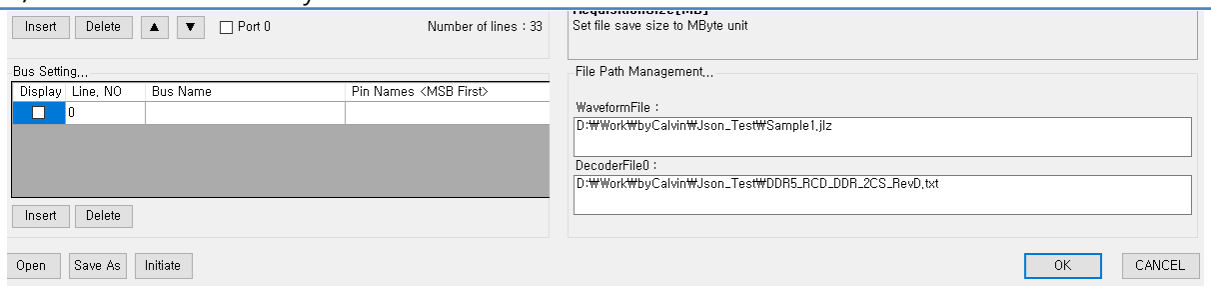
- If you choose "Save as Setup..." from the File Menu, you can save the current settings to a new Setup file
- You can load the settings of the file at desired Setup file through "Open Setup "Open Setup..."





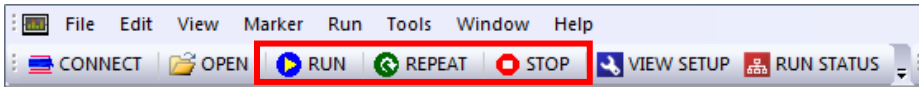
Save Setup & Initiate

- If you click "Open" located at bottom of Setup Window, you can open to already saved setup file.
- If you click "Save AS", it saves current condition at new setup file.(not json file)
- If you click "Initiate", it applies current setting to the system.
- If you click "OK", It maintains current setting but does not save the file.
- If you click "CANCEL", it cancels current setting and restore to previous condition


Insert
Delete
Port 0
Number of lines : 33
Bus Setting...
Display
Line, NO
Bus Name
Pin Names <MSB First>
0
Insert
Delete
Set file save size to MByte unit
File Path Management...
WaveformFile :
D:₩Work₩byCalvin₩Json_Test₩Sample1.jlz
DecoderFile0 :
D:₩Work₩byCalvin₩Json_Test₩DDR5_RCD_DDR_2CS_Rev0.txt
Open
Save As
Initiate
OK
CANCEL

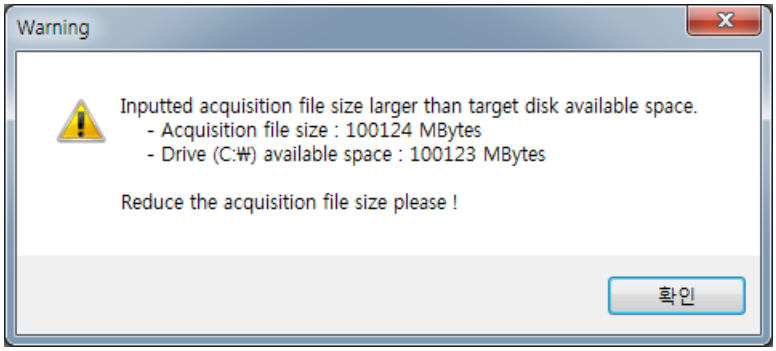
4 Acquisitioning Data from the Device Under Test

4.1 Run / Stop Measurements

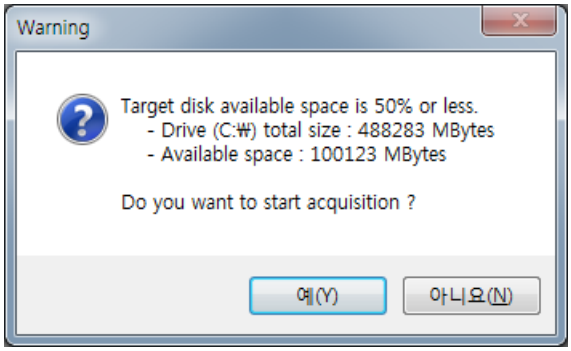


- RUN: Apply current Setup condition to system, and then start acquisition
- REPEAT: Apply current Setup condition to system, and then repeat data acquisition till the user stops it.
- STOP: Stop the current data acquisition. (Acquisition data by the point of STOP is stored in the file)

4.2 Checking Disk Usage

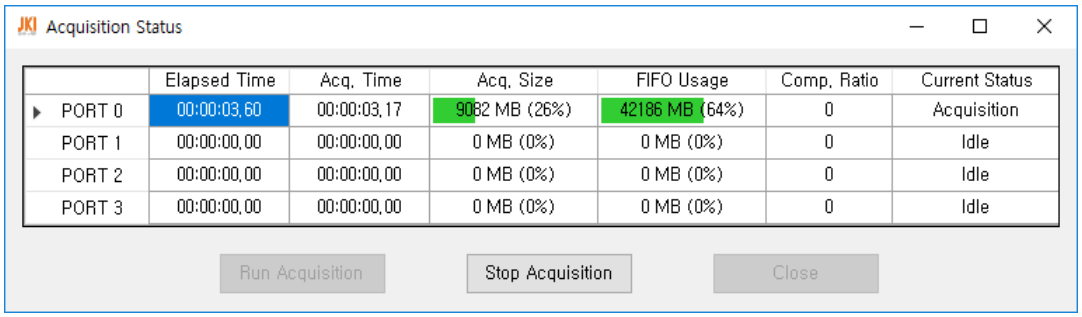


- If the inputted Acquisition Size is larger than the available capacity of the save target drive, an alarm is generated and it is stopped.



- If the save target disk available space is 50% or less, an alarm will appear asking if the acquisition is to proceed.
- Select "Yes", start Acquisition regardless of disk space.
- Select "No", stop Acquisition regardless of disk space.

4.3 Acquisition Status



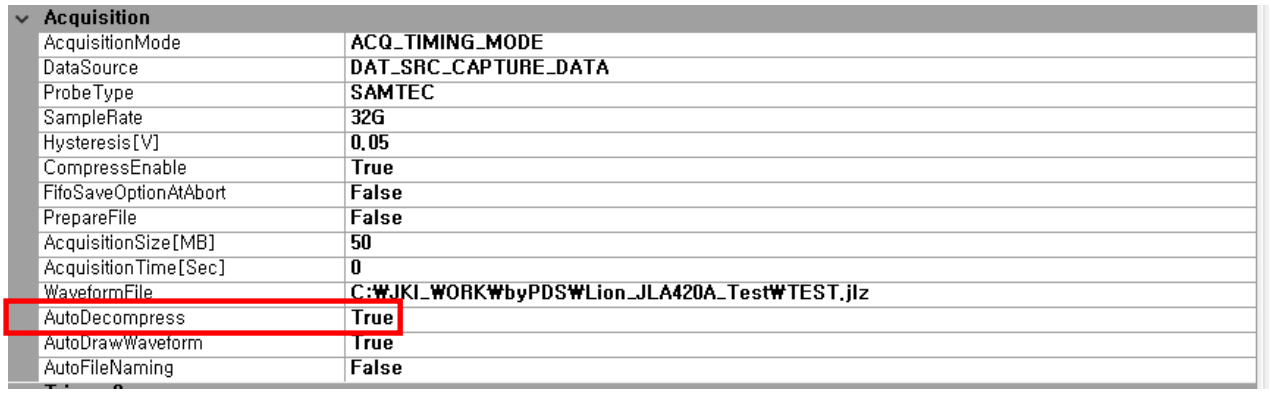
Acquisition Status includes the following items.

Acquisition Status Info

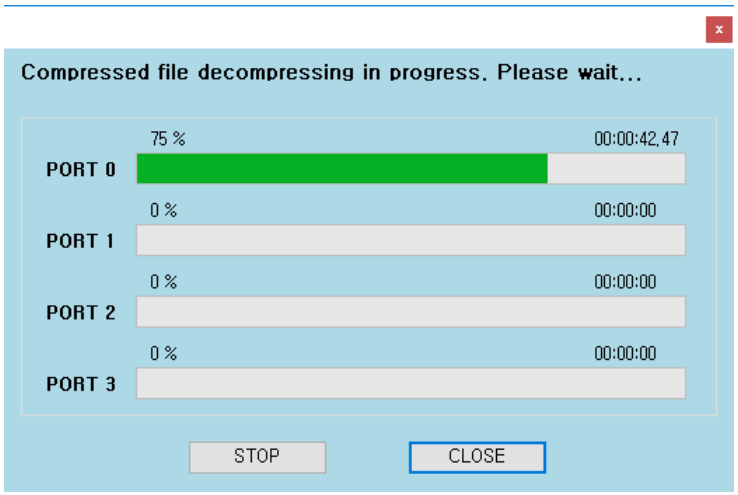
- Elapsed Time: Display the total elapsed time per port after the acquisition
- Acq. Time: Display the total elapsed time per port after on the real acquisition state
- Acq. Size: Display the total acquisition size per port in real time
- (If use the Prepare File mode, it displayed prepared size per port in real time)
- FIFO Usage: Display acquisition memory usage per port in real time
- Comp. Ratio: Indicate Data compression ratio → (input) / (output)
- Current Status: Display the current action status the system per port
- (Idle → Prepare file → Wait for trigger → Acquisition → Flushing FIFO data → Idle)
- Run/Stop Acquisition: You can start new data acquisition or, stop current acquisition.

4.4 Automatic File Decompress

If you set the "AutoDecompress" to True as shown below, automatically decompress file after acquisition.



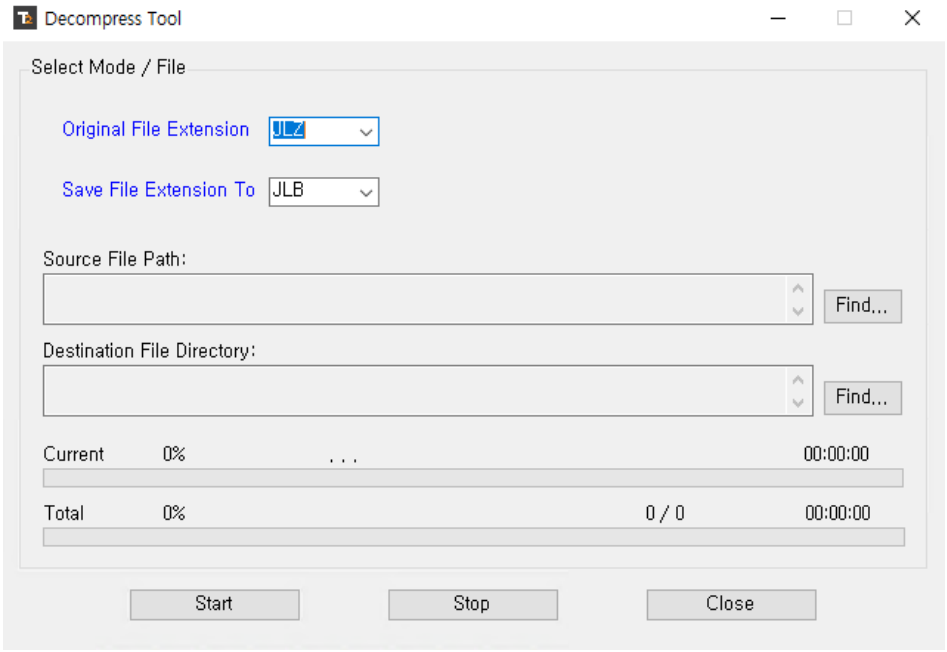
Acquisition	
AcquisitionMode	ACQ_TIMING_MODE
DataSource	DAT_SRC_CAPTURE_DATA
ProbeType	SAMTEC
SampleRate	32G
Hysteresis[V]	0.05
CompressEnable	True
FifoSaveOptionAtAbort	False
PrepareFile	False
AcquisitionSize[MB]	50
AcquisitionTime[Sec]	0
WaveformFile	C:₩JKI_WORK₩byPDS₩Lion_JLA420A_Test₩TEST.jlz
AutoDecompress	True
AutoDrawWaveform	True
AutoFileNaming	False



4.5 Use Decompress Tool

Select "Tools" → "Decompression", it is displayed as below.

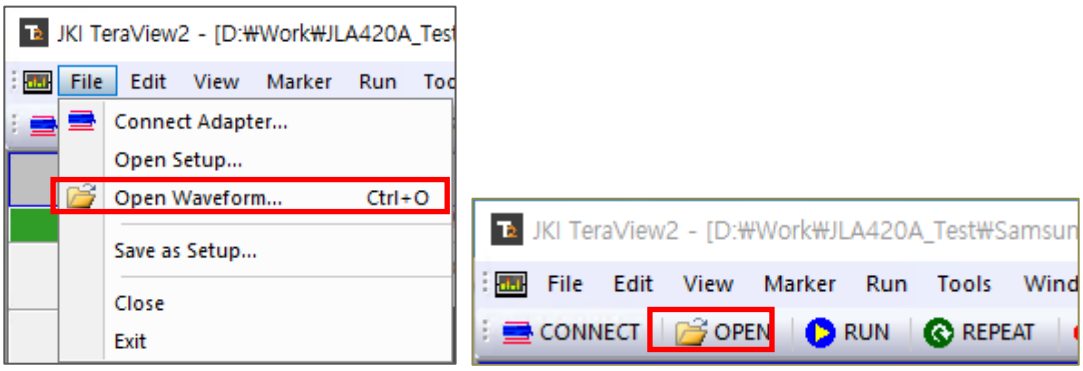
Compressed acquisition data can be decompressed and saved in destination path.



5 Analyzing the Captured Data

5.1 Loading Saved Data

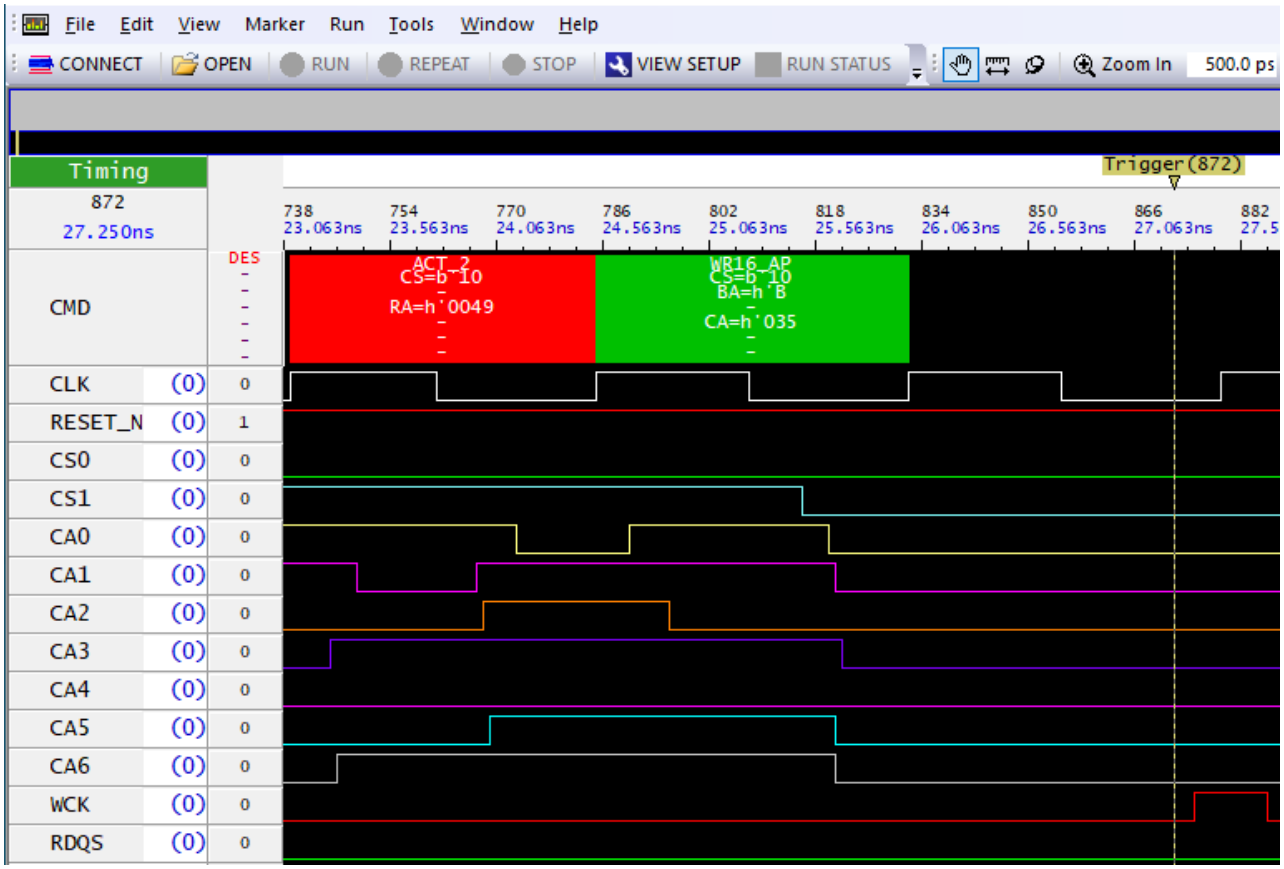
File → Open Waveform File : File Raw data(jlb) is available to open in Open Waveform.



5.2 Analysis Mode

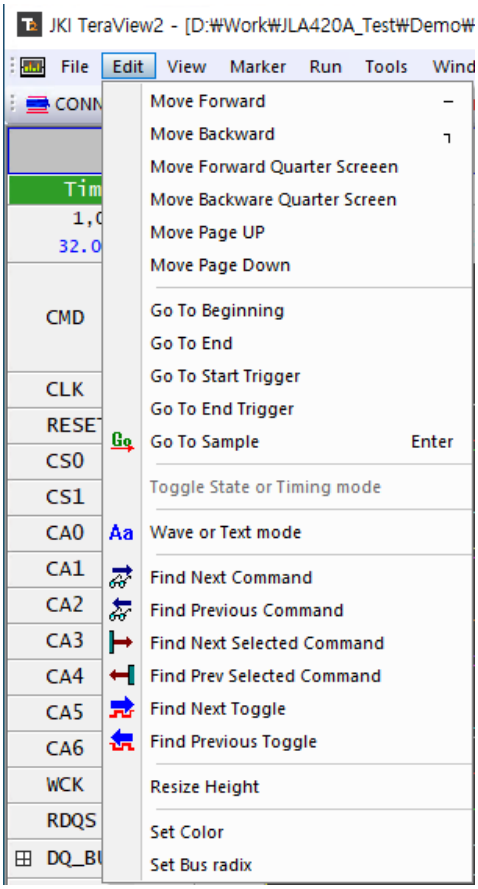
JLA420 supports Timing mode only. (does NOT support State mode)

Timing mode is shown at top left. Ruler shows the Time number as blue at the bottom and the Sample number at the top. The Timing information is drawn in Waveform in Timing mode.



5.3 Navigating Waveform

You can move Waveform through shortcuts or mouse in Edit menu, or screen.



Move Forward

- Shortcut : Ctrl + F
- The function to move Waveform forward as the smallest unit. It moves by 1 sample clock time in timing mode.

Move Backward

- Shortcut: Ctrl + B
- The function to move Waveform backward as the smallest unit. It moves by 1 sample clock time in timing mode.

Move Forward Quarter Screen

- Shortcut: Right arrow
- The function to move Waveform forward by Quarter unit.

Move Backward Quarter Screen

- Shortcut: Left arrow
- The function to move Waveform backwards by Quarter unit.

Move Page Up

- Shortcut: Page Up
- The function to move Waveform backwards from current view by page unit.

Move Page Down

- Shortcut: Page Down
- The function to move Waveform forward from current view by page unit.

Go to Beginning

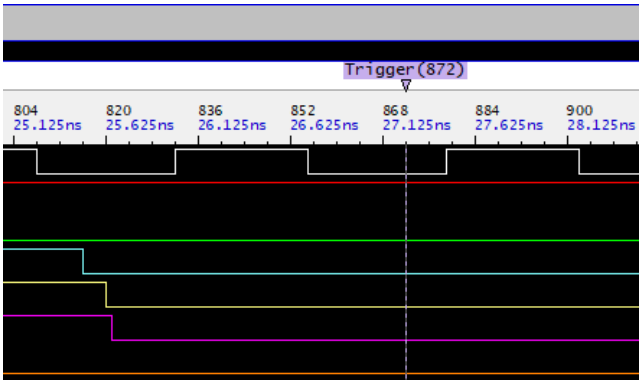
- Shortcut: Home
- The function to move Waveform at the starting point

Go to End

- Shortcut: End
- The function to move Waveform at the last point

Go to Trigger

- After acquisition, You can move into trigger point of view, and then, marks that trigger (Sample) location.



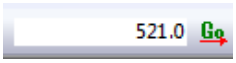
Go to Start Trigger

- Shortcut: None
- The function to move Waveform to Start Trigger point.

Go to Sample

- The function to move Waveform to target sample point
- The method of use is to input Sample or Time value in Tool box at first. Then, clicking "Go button" or "Enter" allows screen to move into specific Sample. Sample value and Time value areas sorted by decimal point. It shows Sample Number if there is no decimal point, shows Time Number if there is decimal point

Sample Number (Input integer)

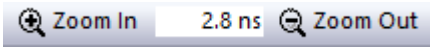


Time Number (Input decimal point)

Scroll

- You can move sample location with mouse drag/press in bottom of Viewer.

Zoom In / Out



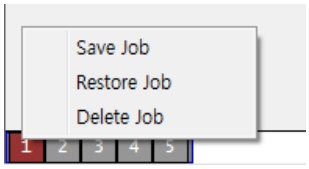
- Zoom In – Shortcut : Shift + I
- Zoom Out – Shortcut: Shift + O
- You can Zoom In / Zoom Out with the button shown in the above.
- Drawing quadrangle with left mouse button zooms in corresponding area in Waveform screen.

Copy Sample or Time

- Sample Number and Time Number are shown at the top left. Copy pop-up appears by clicking this area. "Copy Sample" copies Sample number and "Copy Time" copies Time number. "Copy All" copies all of Sample and Time value and separates Sample Time value with Space character.

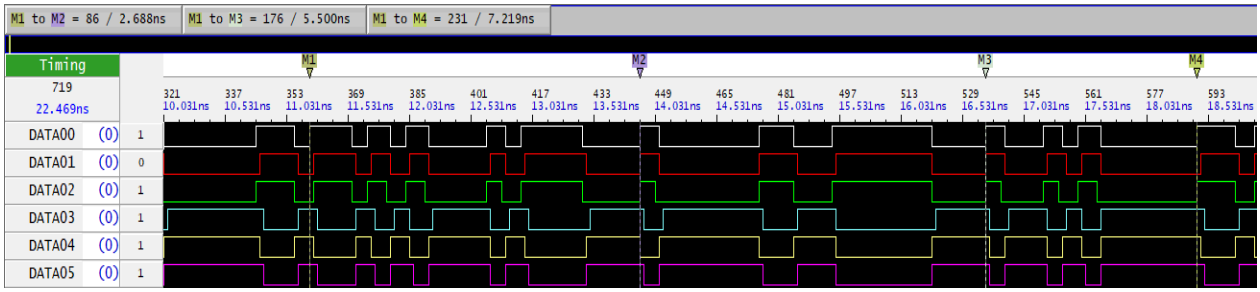
Save Current Screen

- Save/Restore Job function located at the bottom left allows to save Waveform screen into program and to restore the file up to five screens. Pop-up menu appears by clicking mouse right button on certain numbers as shown in the bottom picture. It saves at certain number by clicking "Save Job", and it moves to the saved screen by clicking Restore Job or double click.



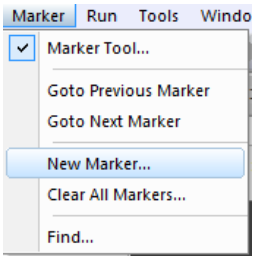
5.4 Marker

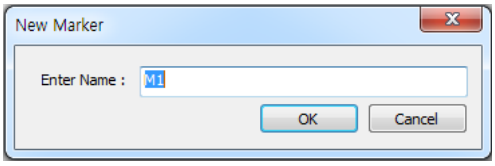
- Marker function is to show or to move into location of Waveform.



New Marker

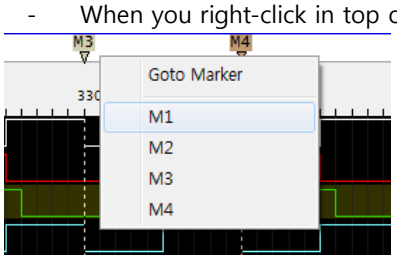
- Double click Marker bar area at the top of Ruler or Run Marker -> New Marker from Menu or Tool bar  creates new Marker. You can drag created Marker to move into desired position.





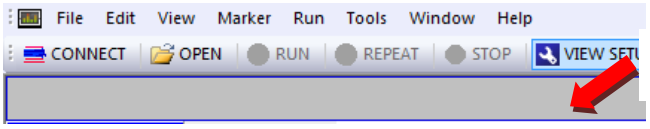
Goto Marker

- When you right-click in top of the sample position, Marker list pops up as shown below.



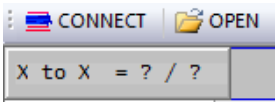
Marker Tool

- Marker Tool is created if you click "Marker -> Marker Tool" from Menu or Tool bar. 

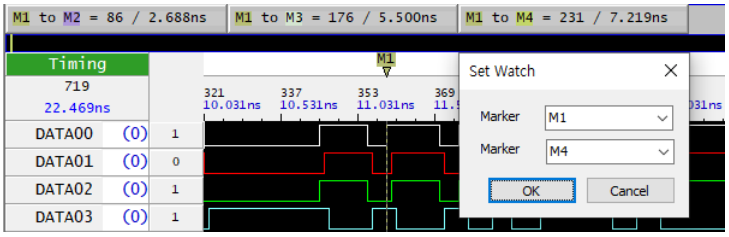


Double Click

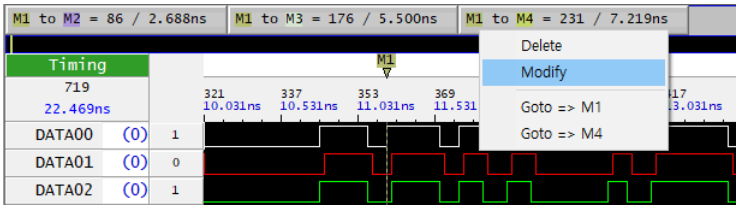
- Tool box is created if you double click or right-click of Marker Tool area.



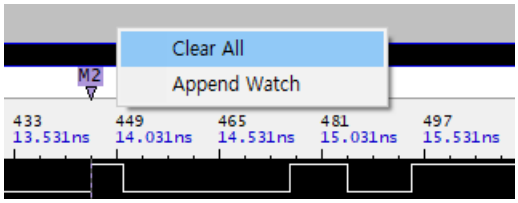
- Double click Tool box as shown above first. Then, the window, which appoints two Markers, pops up as shown below. After that, inputs number of sample and Time information between Markers.



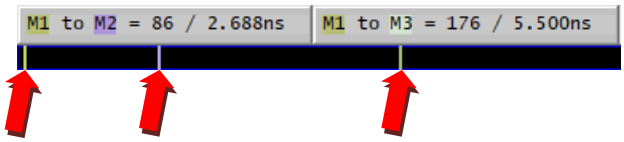
- Right-click of the window allows using "Delete", "Modify", and "Goto Marker" functions.



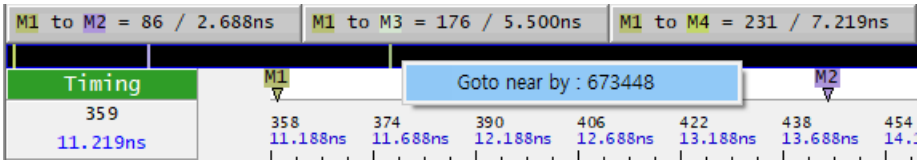
- Right-click of Marker Tool area to use "Clear All" function, which deletes all.



- In the black area below, you can see the approximate distribution of the marker for the entire waveform area.



- If you double-click or right-click the mouse, you can move to the nearby sample location as follows.

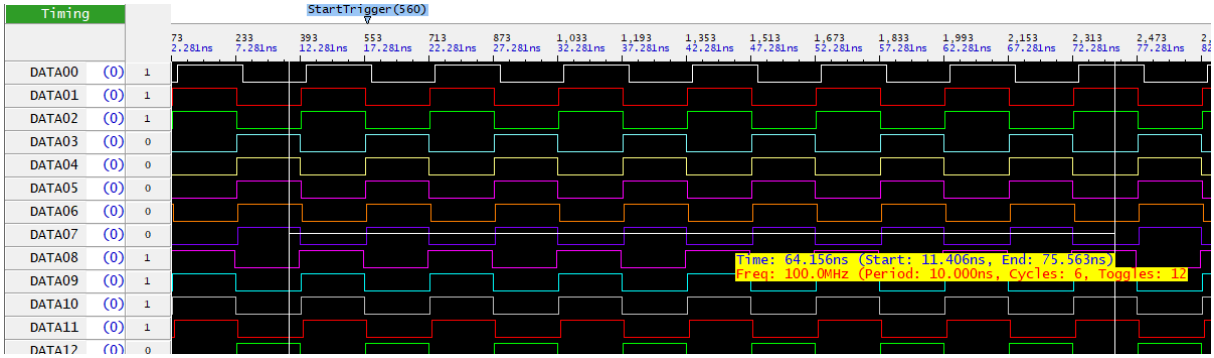


5.5 Ruler

You should select CH you want to measure first.

Two places' information is displayed after dragging two places by clicking  Ruler icon.

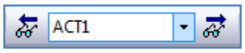
- First line - Time interval
- Second line – Frequency, Period, Cycle, Toggles



5.6 Toggle Search

You can find previous or next points of signal toggle by clicking two-way arrow as shown above.

5.7 Command Search



All command appears by loading command file from Packet decoder. Select desired command and click either left arrow to move previous Waveform screen or right arrow to move next Waveform screen.

5.8 Selected Command Search

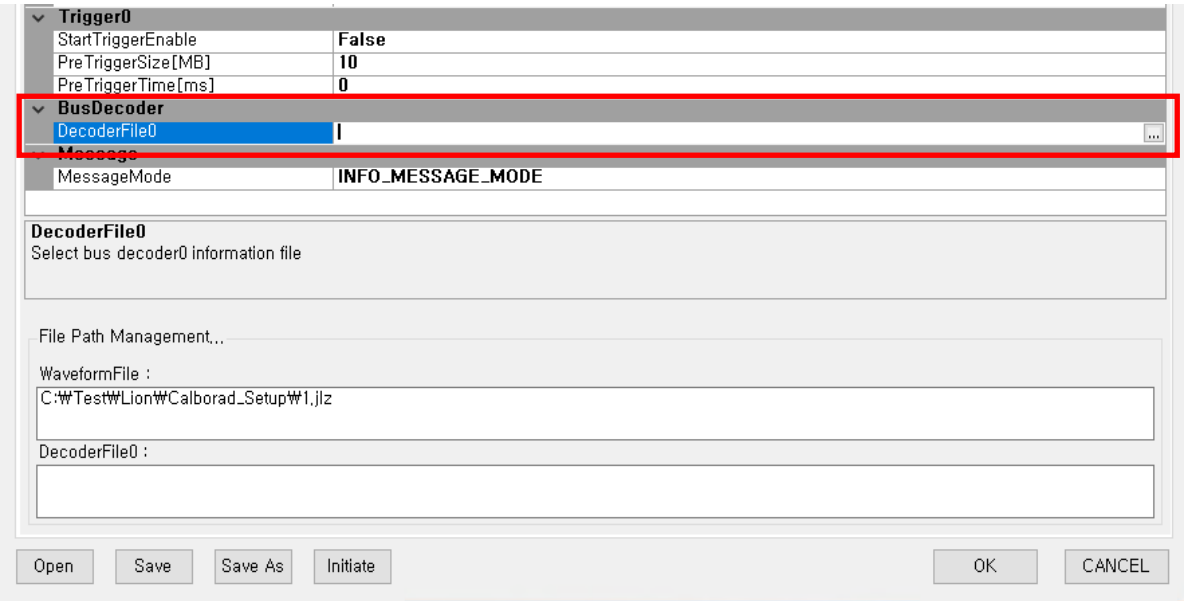
You can find previous or next same command by clicking two-way arrow you selected desired command.

5.9 Bus Decoder

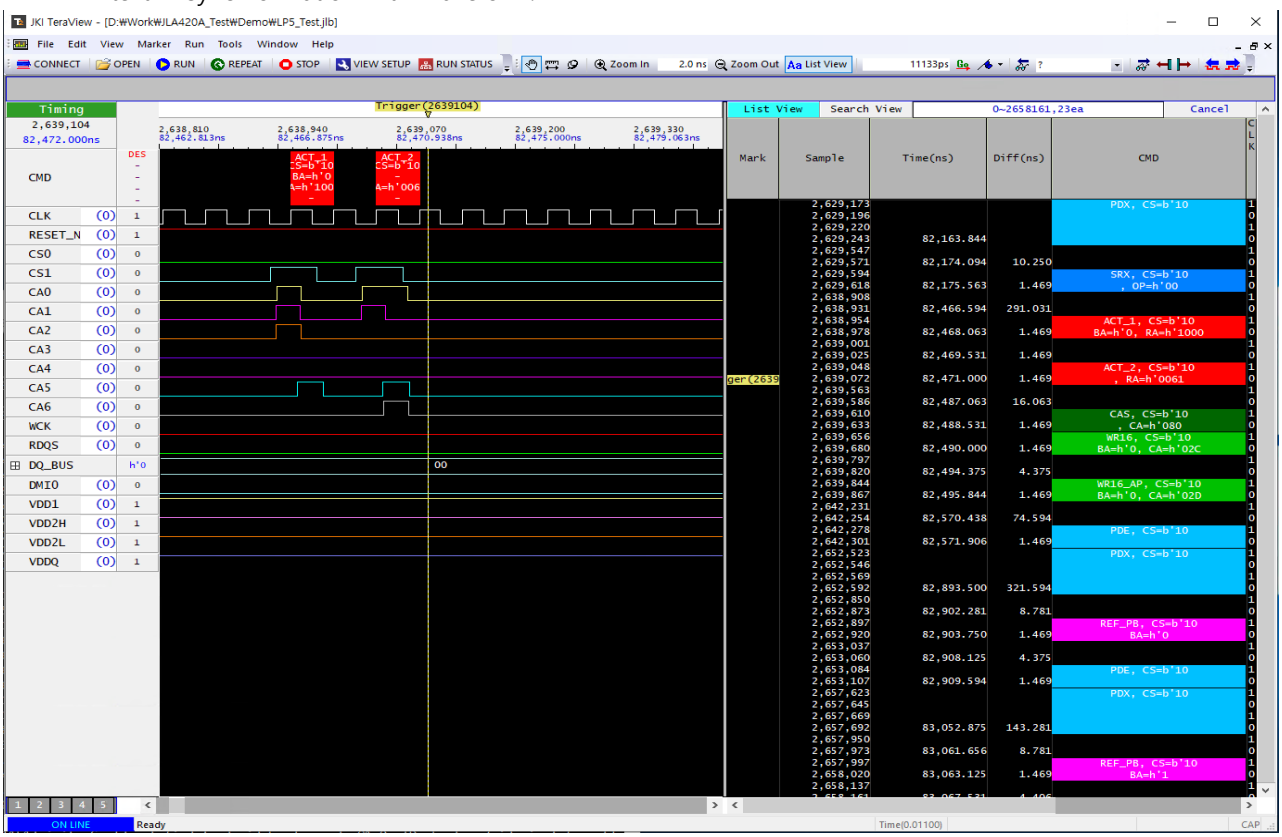
To decode memory bus protocol, we provide pre-defined decoder files for various JEDEC standard memory types.

How to use

- VIEW SETUP → Option tab.
- Select pre-defined decoder file → Click "OK"button.



- If you click the button Aa List View on the top menu, ListView is created horizontally on the right side of Waveform, and as shown above, all Sampling data and Command information can be viewed based on text in synchronization with Waveform.



6 Reference

6.1 System Specification

Channel Specification	
Number of Channels	34 (31 single-ended + 3 differential)
Input Voltage Range	-0.2V to 1.2V (analyzer input)
Minimum Input Voltage Swing	40 mV (analyzer input)
Termination (Vtt) Voltage Range	0V to 1.2V (analyzer input)
Termination (Vtt) Voltage Resolution	1 mV
Threshold (Vref) Voltage Range	0V to 1.2V (analyzer input)
Threshold (Vref) Voltage Resolution	1 mV
Hysteresis (Vhys) Voltage Range	0 ~ 50 mV
Timing Delay Range	-2ns to 2ns
Timing Delay Resolution	31.25 ps @32 GHz
Input Impedance	50 Ohm (analyzer input) 250 Ohm (5:1 probe) 500 Ohm (10:1 probe)

Acquisition Specification	
Sample Rate	2 / 4 / 8 / 16 / 32 GHz
Analysis Mode	Timing mode, Eye mode
Acquisition Memory	Max. 512 GB (standard 128 GB)
Host Interface	PCIe Gen3 x8
Data Compression	Hardware compression
Data De-compression	Software de-compression

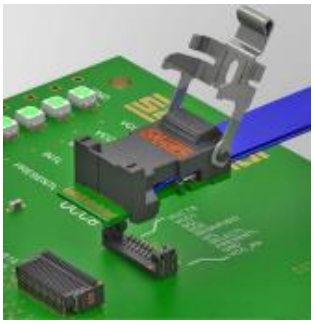
Trigger Specification	
Trigger Pattern	E(Either edge), R(Rising edge), F(Falling edge), H(High), L(Low), X(Don't care) for all channel
Trigger Sequence	5 burst trigger
Trigger Action	Start capture
Trigger Rate	2G
Pre-trigger Size	Max. 128Gbytes (depends on RDIMM size)

Environmental and physical	
Power Consumption	Max. 150W
Operation Temperature (nom)	0 to +40 dec C
Humidity (nom)	0 to 80% relative humidity
Dimensions (W x H x D)	347 mm x 290 mm x 74 mm
Weight	4.7kg

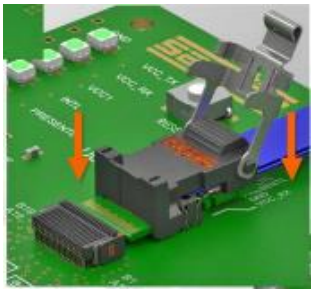
6.2 Probe Connector Pin-outs (Samtec)

Samtec Probe Connector Pin-map					
Channel#	**Description**	**Pin#**	**Pin#**	**Channel#**	**Description**
GND	Ground	1	2	GND	Ground
CH_22	Data Channel	3	4	CH_23	Data Channel
GND	Ground	5	6	GND	Ground
Reserved	Not connect	7	8	CH_24	Data Channel
GND	Ground	9	10	GND	Ground
CH_21	Data Channel	11	12	Reserved	Not connect
GND	Ground	13	14	GND	Ground
CH_20	Data Channel	15	16	CH_25	Data Channel
GND	Ground	17	18	GND	Ground
Reserved	Not connect	19	20	Reserved	Not connect
GND	Ground	21	22	GND	Ground
CH_19	Data Channel	23	24	CH_26	Data Channel
GND	Ground	25	26	GND	Ground
CH_18	Data Channel	27	28	CH_27+	Differential+ or single-ended
GND	Ground	29	30	GND	Ground
Reserved	Not connect	31	32	CH_27- / NC	Differential- or not-connect
GND	Ground	33	34	GND	Ground
CH_17	Data Channel	35	36	Reserved	Not connect
GND	Ground	37	38	GND	Ground
CH_16	Data Channel	39	40	CH_28	Data Channel
GND	Ground	41	42	GND	Ground
CH_31	Data Channel	43	44	CH_29	Data Channel
GND	Ground	45	46	GND	Ground
CH_15	Data Channel	47	48	Reserved	Not connect
GND	Ground	49	50	GND	Ground
CH_08	Data Channel	51	52	CH_30	Data Channel
GND	Ground	53	54	GND	Ground
Reserved	Not connect	55	56	CH_07	Data Channel
GND	Ground	57	58	GND	Ground
CH_09	Data Channel	59	60	Reserved	Not connect
GND	Ground	61	62	GND	Ground
CH_10	Data Channel	63	64	CH_06	Data Channel
GND	Ground	65	66	GND	Ground
CH_11- / NC	Differential- or not-connect	67	68	ETC_ADC0	Voltage monitoring
GND	Ground	69	70	GND	Ground
CH_11+	Differential+ or single-ended	71	72	CH_05	Data Channel
GND	Ground	73	74	GND	Ground
CH_12	Data Channel	75	76	CH_04	Data Channel
GND	Ground	77	78	GND	Ground
CH_13	Data Channel	79	80	ETC_ADC1	Voltage monitoring
GND	Ground	81	82	GND	Ground
CH_32	Data Channel	83	84	CH_03	Data Channel
GND	Ground	85	86	GND	Ground
ETC_ADC2	Voltage monitoring	87	88	CH_02	Data Channel
GND	Ground	89	90	GND	Ground
**CH_33-	Dedicated Clock- (Diff)	91	92	CH_01	Data Channel
GND	Ground	93	94	GND	Ground
**CH_33+	Dedicated Clock+ (Diff)	95	96	CH_00	Data Channel
GND	Ground	97	98	GND	Ground
ETC_ADC3	Voltage monitoring	99	100	CH_14	Data Channel

6.3 Probe Module Cable Assembly Insertion and Removal Instructions

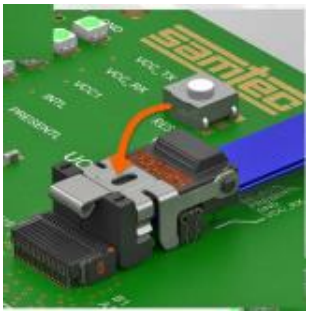


1. Align optical or copper assembly so that notches in PCB are over the positive latching receptacle.

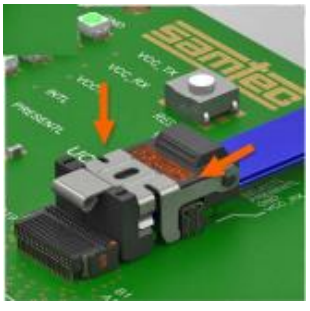


2. Drop cable assembly down keeping it parallel to the board.

3. Slide cable assembly forward until engaged, keeping it level with the board.

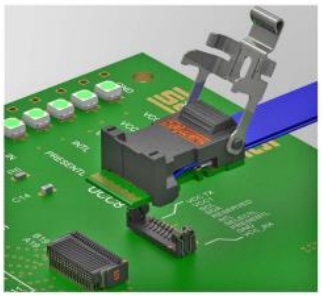


4. Rotate latch downwards until parallel to board.

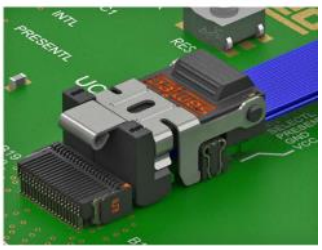


5. Depress latch to lock cable assembly into the connector. Removal is reverse of installation.

Unmated (Latch Open)



Mated (Latch Down)



6.4 Warranty & Calibration Service

Warranty: JLA420A DDR5/LPDDR5 protocol analyzer is provided with 1 year warranty.

Calibration:

- The JLA420A protocol analyzer does not require an operational accuracy calibration or adjustment.
- Instead of that, We provide protocol analyzer's performance/functionality test every 3 years.
- We recommend you to take protocol analyzer's performance/functionality test every 3 years
- The 1st 3 years test service is no charge. Then need to pay for this test service.

  *For more details, Contact sales@jkic.co.kr