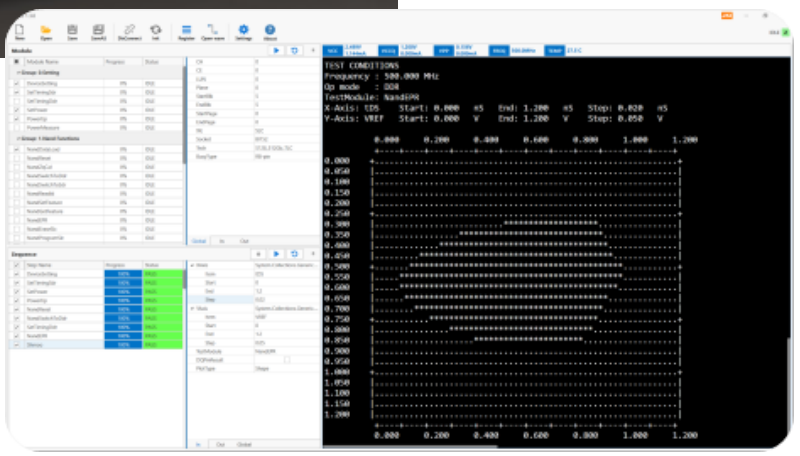
JKI NAND Engineering Tester

User Manual

Applicable Product: JTS350F, JTS351F



Version 2.0

JKI Inc.

Version History

Version	Date	Remarks
1.0	2021-10-15	Draft release.
2.0	2022-07-26	Renewal manual.

Contents

1. Overview

1.1. Description

JKI's high speed NAND tester delivers high performance with affordable price and small size for testing next generation high speed NAND flash memories. This NAND tester is a portable size engineering test solution developed based on the latest MPSoC + FPGA technology. It supports 2.4Gbps interface using high speed DDR I/O and provides multi-channel programmable precision device power supplies.

<JTS350F>

<JTS351F>

1.2. Features

Fast Control & Easy Development

- Fast MPSoC based test controller (ARM + FPGA)
- Easy test program development environment on Linux
- Easy sequence & parameter control environment on Windows

Software-defined Pattern Generator

- Software-defined command & data pattern generation
- Continuously streaming write and read data vector

Hardware-based Timing Generator

- Support 64 user defined timing sets
- Support source synchronous clocking

Programmable AC/DC Parameter

- Programmable power supplies (8 power sources)
- Programmable test speed up to 2400 Mbps (DDR)
- Programmable AC parameters

Best Signal Integrity

- Best signal integrity for high speed I/Os (HSIO)
- Additional general purpose I/Os (GPIO)

Applications

- Engineering test solution for high-speed DDR NAND devices
- NAND flash memory design validation, characterization and failure analysis

1.3. Included Components

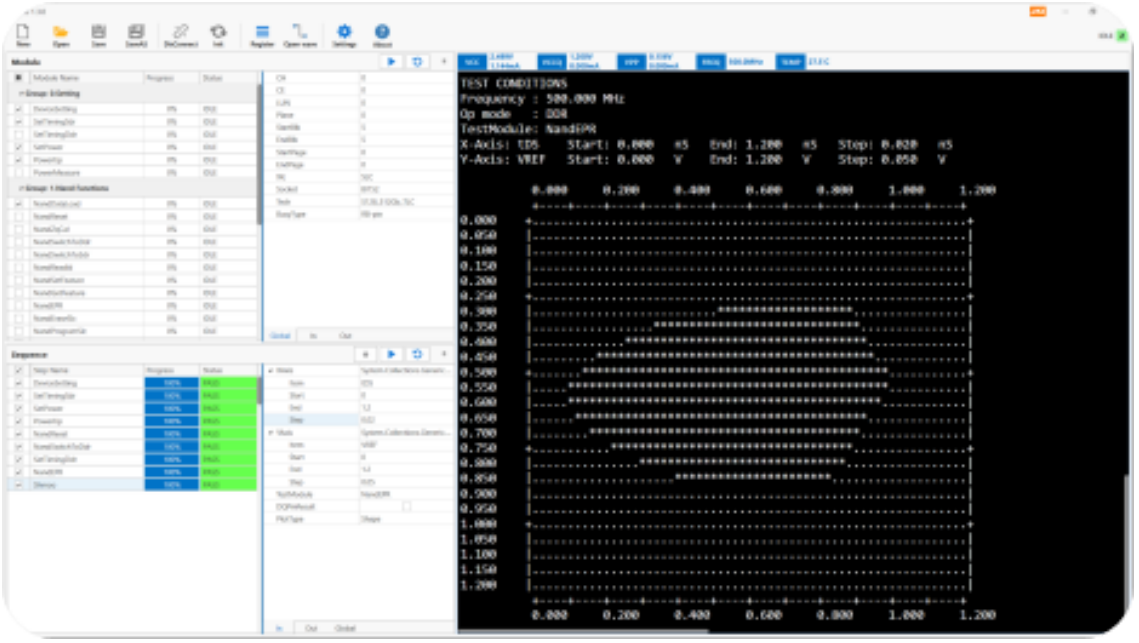
The components of tester kits are as follows.

1) NAND Engineering Tester
2) Socket Board (not included in basic configuration, sold separately)
3) USB Ethernet Adapter
4) Ethernet Cable
5) AC/DC Power Adapter
6) Test Automation Studio Software (via download link)
7) Test Pattern Programming SDK (via download link)

2. Software Installation

2.1. Download

The Test Automation Studio Software (named PAS) is provided free of charge and can be installed on as many machines as you want. The latest release of the PAS software can be downloaded via the given download link.
The PAS software can manage test modules, test parameters and test sequences with automated synchronization capability with NAND test pattern software development kit (SDK) which is running on embedded O/S in the target test system.



2.2. Supported Operating Systems

The PAS software is supported in the following operating systems.

- Windows 7 (x86/64)
- Windows 10 (x86/64)
- Windows 11 (x86/64)

2.3. Installation

No installation process is required, just unzip the provided compressed file and copy it to any folder.

2.4. Firmware Update

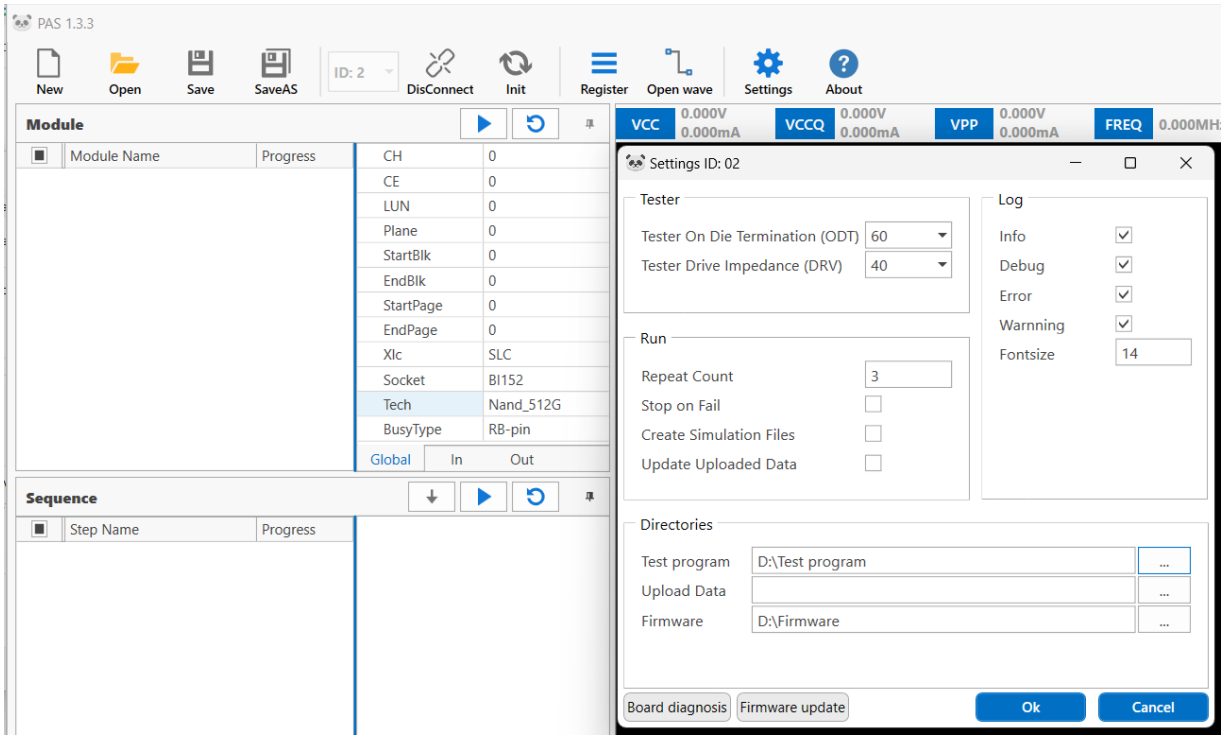
If you need to update the firmware such as bug fixes, you can update the firmware through the PAS software.

Precautions

- Do not operate/change the power or USB/Ethernet connection during the update.
- The update process takes about 10 seconds to complete.
- The firmware works with proper S/W version, so avoid using mixed versions.

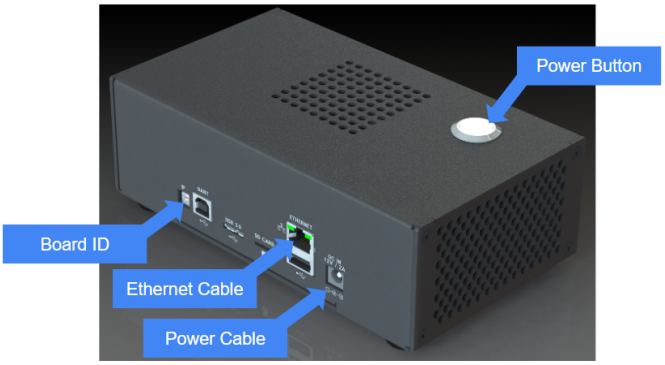
How to update

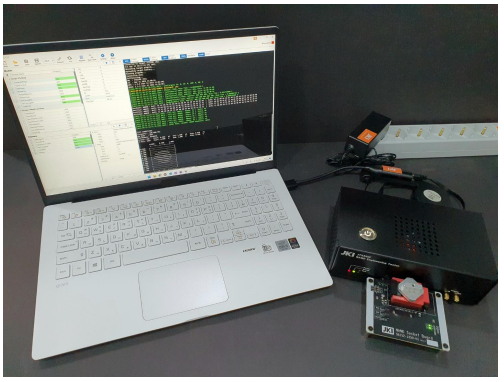
- Select the ID of the target tester. And click the “Connect” button.
- When the connection is complete, click the “Settings” button.
- Specify the path where the new firmware file is located in the “Directories>Firmware” item in the Setting window.
- Press the “Firmware update” button.
- While the update is in progress, you can check the progress and completion status in the main log window.
- If the update fails due to power failure or Ethernet disconnection while attempting to update, try again from the beginning.
- Press the “Init” button to load the new firmware. The firmware version can be checked in the main log.



3. Getting Started

3.1. Setup





Connect Power Cable

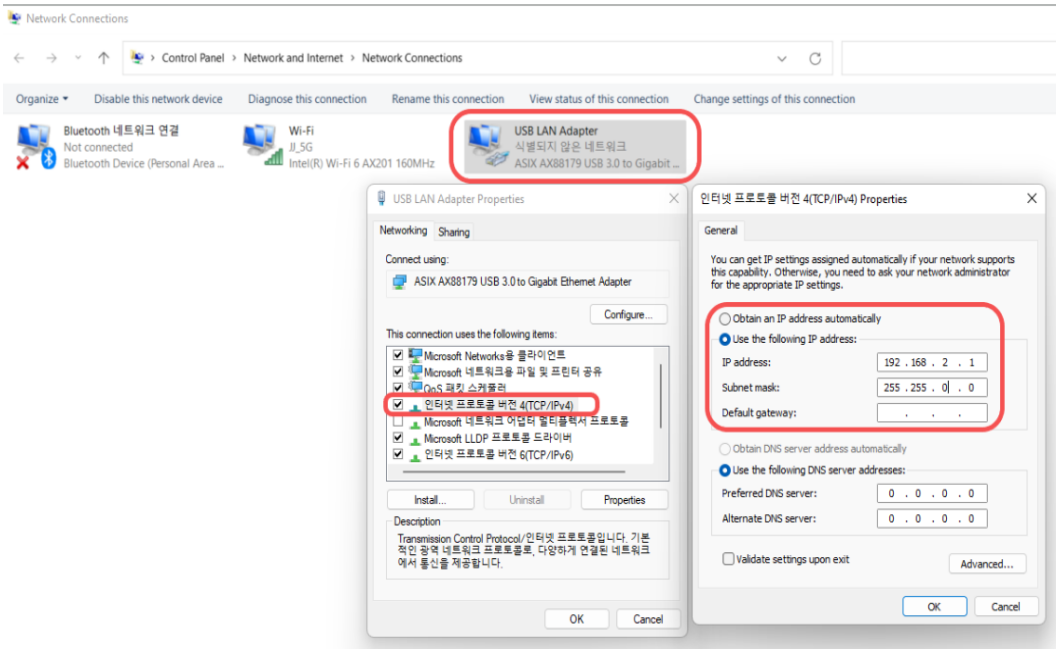
Connect the 12V adapter to the DC IN terminal on the back side.

Connect Ethernet Adapter & Cable

Connect the Ethernet adapter and cable to the rear Ethernet terminal.

Network Setting on PC

- Network Settings: Select the adapter or LAN card connected to the tester in "Control Panel\Network and Internet\Network Connections".
- Set the IP and subnet mask of Ethernet protocol version4 in the properties as follows.
    - IP address : 192.168.2.1
    - Subnet mask : 255.255.0.0
    - Default gateway: 192.168.2.1



Set Tester ID

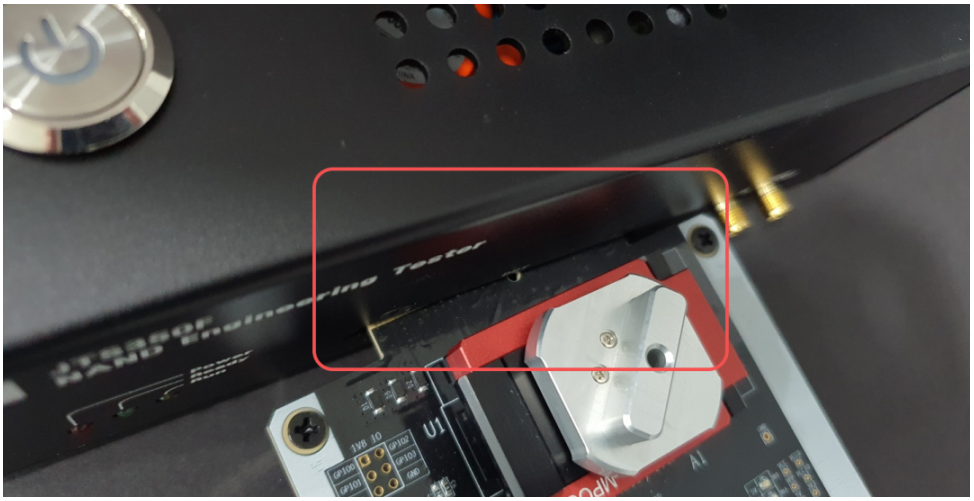
The last number of the IP address is matched with the rotary switch on the back of the tester. (Adjustable from 0 to 7)

Connect Socket Board

CAUTION: Be sure to connect the DUT board when the power is off.
CAUTION: Push in the DUT board until it is fully engaged.

- Correct example

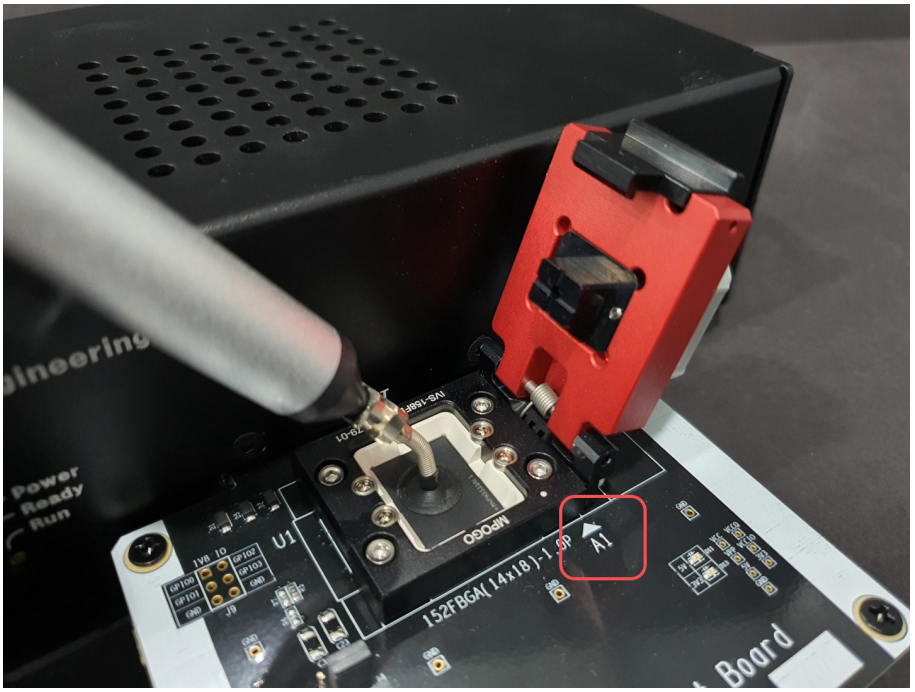
- Incorrect example



Load the Device

CAUTION: Be sure to install the device with the power off.
CAUTION: Turn the dial fully counterclockwise before opening.

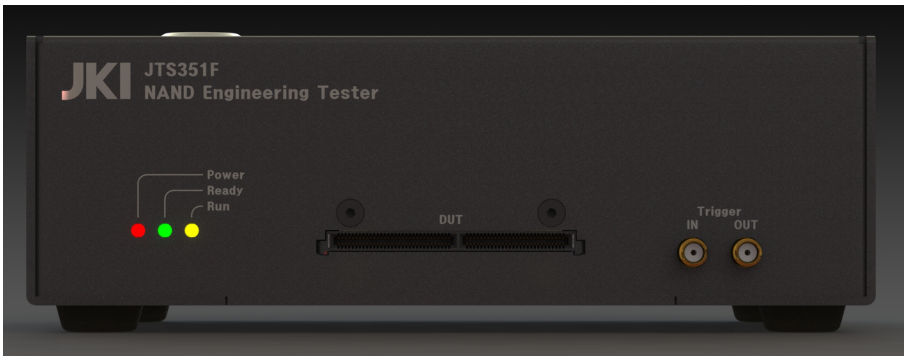
1) Open the socket cover.
2) Place the NAND in the direction of the A1 mark.
3) Tighten the dial clockwise to match the height of the device.



3.2. Initiate

1. Turn on the instrument's power switch
2. Make sure the status LED is turned on and the LED will be lit Red.
3. Start the PAS software.
4. Select device ID and target test program path in the Setting window.
5. Click "Connect" button
6. Click "Init" button

    - Power: Power on
    - Ready: Ready to connect
    - Run: Blinks during the RUN operation



3.3. Configure

Edit Module, Sequence, Parameters or open Sequence to edit test items.
Refer to Managing Test Modules, Parameters and Sequence

3.4. Run

Click the Run, Repeat Run button at the top right of the Module or Sequence to proceed with the test. Refer to Running Modes

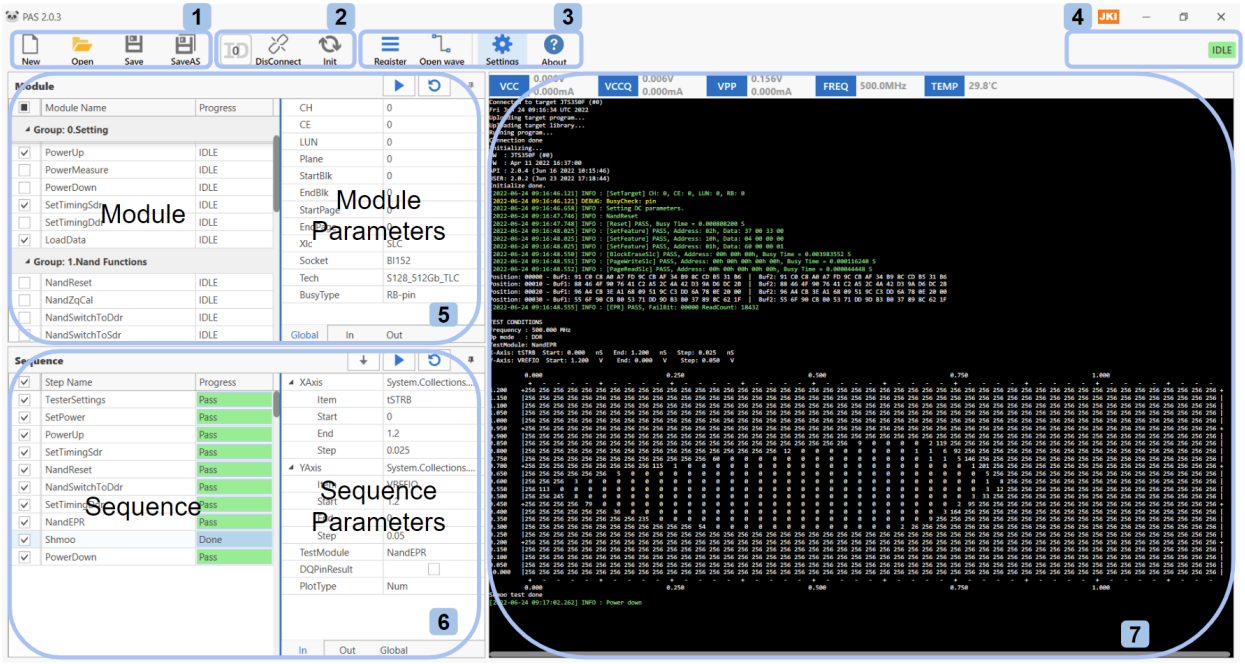
3.5. Verify

The progress and results of the test program are displayed in log windows.

4. Using the Software

4.1. Navigating the Software

The PAS software consists of the following sections.



Setting

- The Settings window edits and saves the overall settings of the system.

Module

- The test module panel shows the list of test modules written by the user and input/output parameters for each module.

Sequence

- In the sequence panel, the user can drag and drop test modules, list them in the desired order, and change the parameters for each step to execute.

Running

- The user can select individual or multiple modules to run once or repeatedly.

Logging

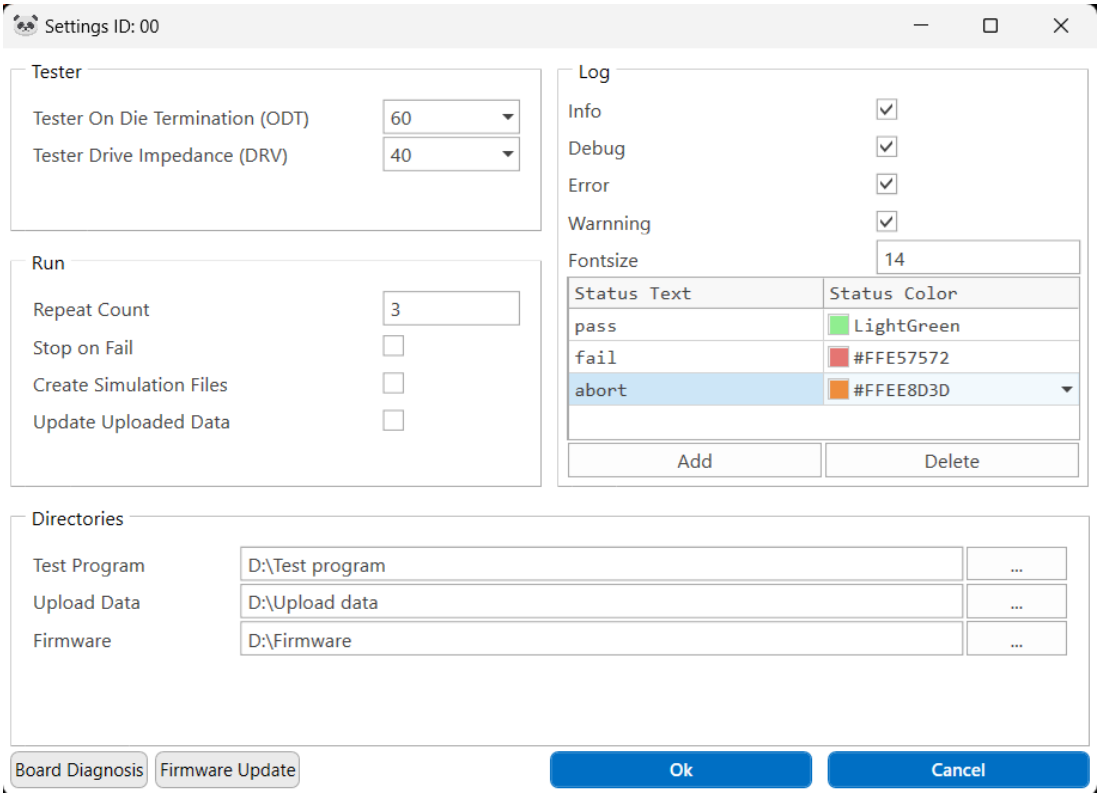
- The log panel displays all standard output messages from user code.
- It also displays the voltage, current, frequency and temperature on board.

Tools

- The Register tool provides the ability to read and write a set of device register information from a CSV file in one step.
- The Wave tool shows a simulated waveform of how the test pattern is actually created.

4.2. Configuring Tester Settings

The Settings window edits and saves the overall settings of the system.



Tester Settings

- Tester On Die Termination (ODT) : Select the On Die Termination (ODT)value of the tester
- Tester Drive Impedance (DRV) : Select the Drive Impedance(Strength) value of the tester

Run Options

- Repeat Count: Specifies the number of repeat counts for the Repeat Run.
- Stop on Fail: Select whether to stop when failure occurs upon Running.
- Create Simulation Files: Select whether to save the simulation waveform upon Running.
- Update Uploaded Data: Select whether to update Upload Data files to target upon Connecting.

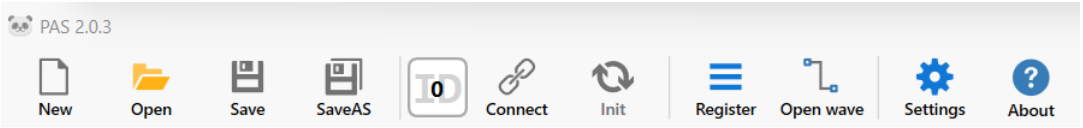
Log Options

- Select the log level to be displayed in the log window and adjust the font size.
- Specifies the background color of the status string in the Progress column.

Directories

- Target Program : The path of test program and JKI Library file built from SDK.
- Upload Data : The path of user's data to upload (target path : /tmp/user)
- Firmware : The path of firmware files

4.3. Connecting the Tester



- If the user clicks the Connect button after entering the target ID, the test program and user's upload data is uploaded to target automatically.
- The user can check the progress and completion status in the main log window.
- When Connect is completed, the GlobalParameter item is listed in the Module Parameters Global tab and the Init button is activated.

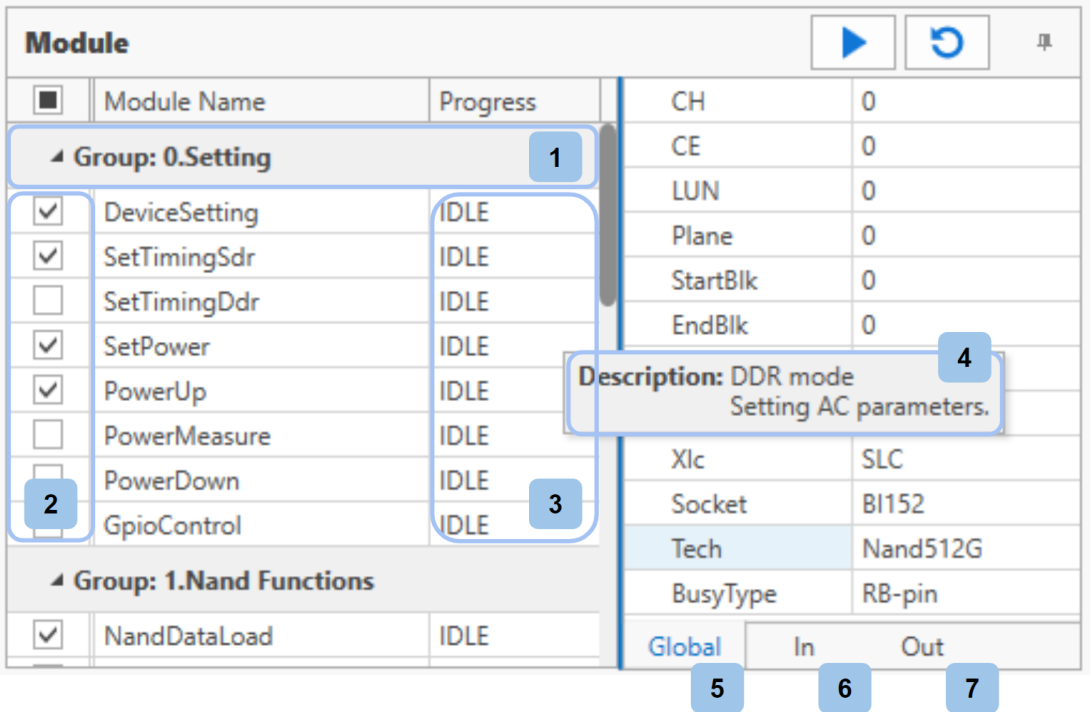
4.4. Initializing the Tester

- Click Init button for initialization of tester
- The user can check the progress and completion status in the main log window.
- When initialization is completed, the test modules registered in the test program are listed in the Module window.

4.5. Managing Test Modules, Parameters and Sequence

Test Module

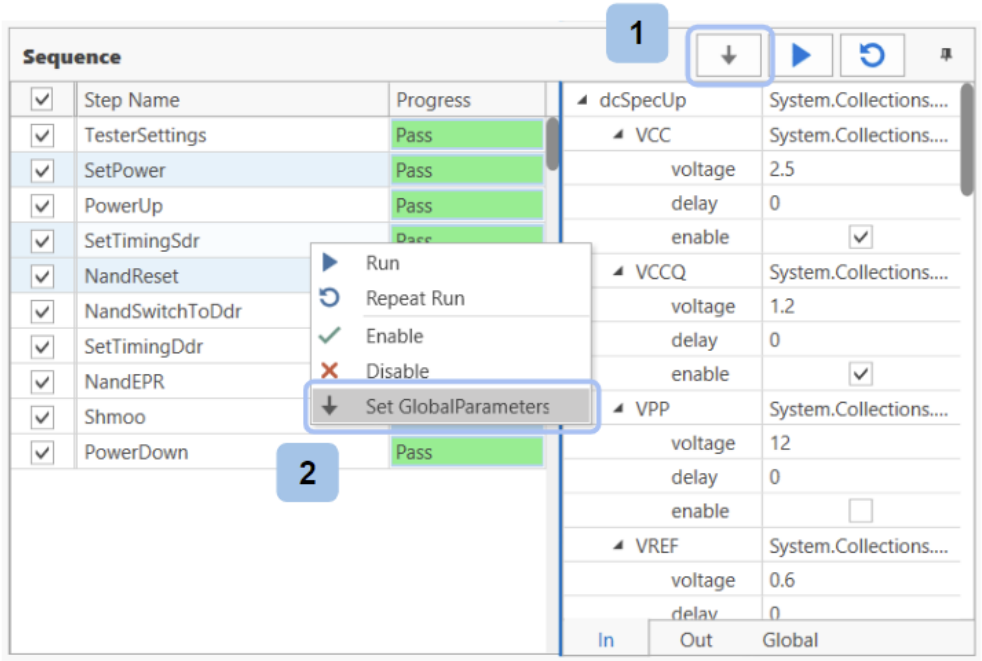
The test module panel shows the list of test modules written by the user and input/output parameters for each module.



1 Group: the group of test modules (automatically sorted in alphabetical order)
2 Check Box: enable or disable for Running
3 Progress & Status: Progress bar and Status text is displayed
4 Description: When the mouse is over, it displays the Description tooltip
5 Global parameter: Global variables used globally across all test modules
6 Input parameter: Input local variables used in each test module
7 Output parameter: Output local variables used in each test module

Sequence

In the sequence panel, the user can drag and drop test modules, list them in the desired order, and change the parameters for each step to execute.

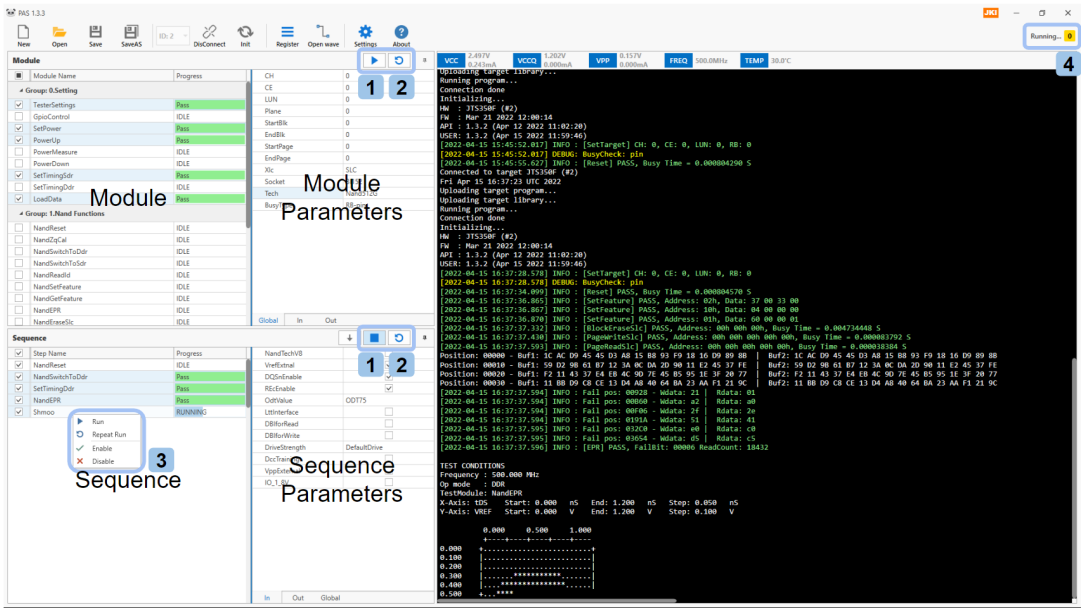


- All input/output/global variables in the sequence panel are local variables for each step. Therefore, the user can set different settings for each step.
- If you want to bring global variables from the test module panel to each step in the sequence panel, click button 1 to apply them all, or right-click each step and click 2 Set GlobalParameters.
- Each step name can be edited by double-clicking it.
- Users can change the module order using drag and drop or shortcut keys.
- Users can copy or paste modules using shortcut keys. In the case of paste, it is pasted under the selected module.
- Modules can be deleted using hotkeys.

4.6. Running Modes

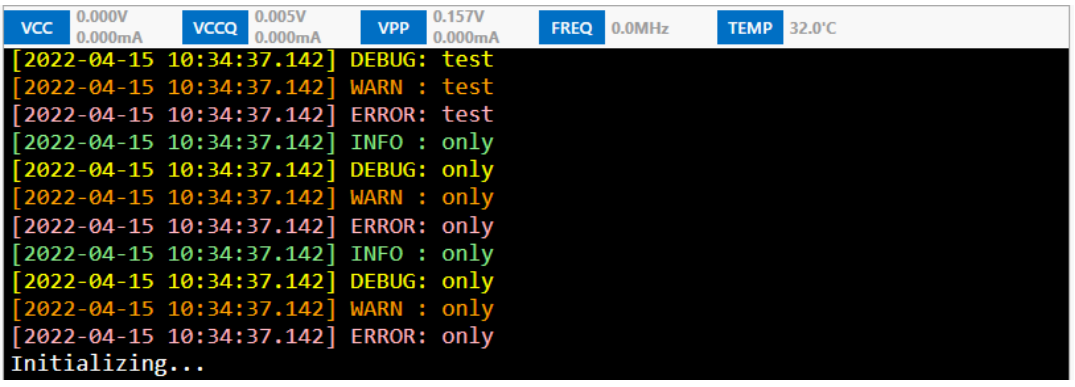
Several execution methods are provided in the test module panel and sequence panel.
The user can select individual or multiple modules to run once or repeatedly.

1 Single Run
2 Repeat Run
3 right-click menu : Run, Repeat Run
4 Repeat Run Count : the number of times currently running



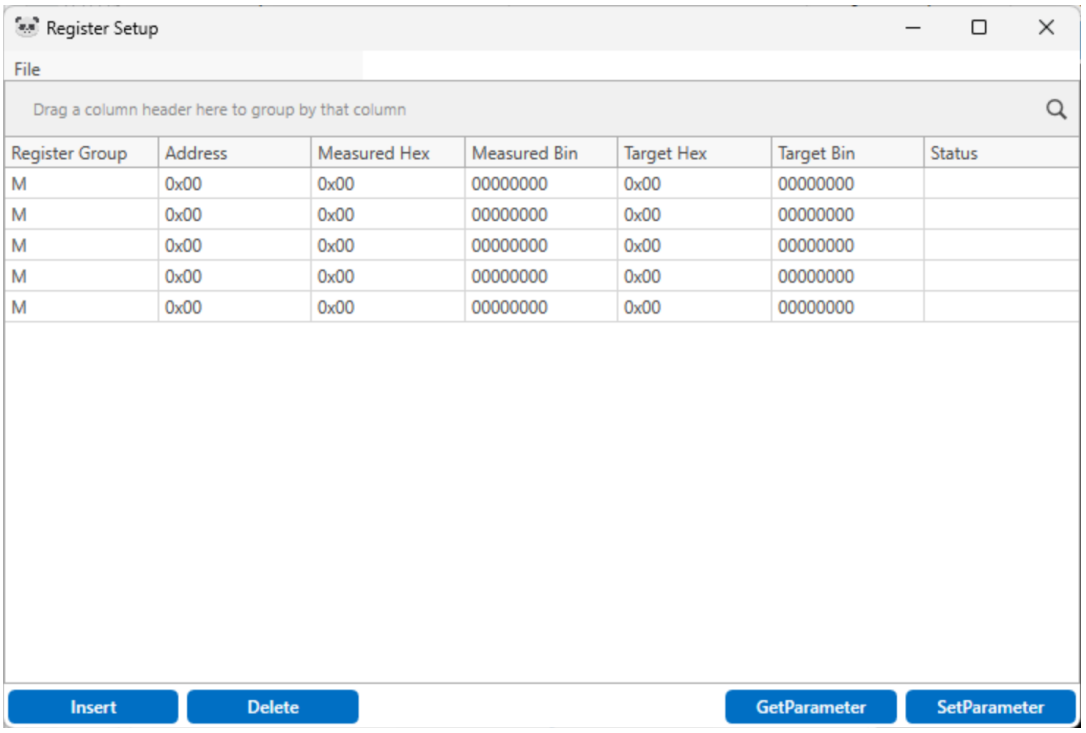
4.7. Verifying Test Result

The log panel displays all standard output messages from user code.
It also displays the voltage, current, frequency and temperature on board.
It is automatically written to the log file according to the date and different colors are supported according to the log level.



4.8. Using Register Setup

The Register setup tool provides the ability to read and write a set of device register information from a CSV file in one step.



Editing

- Insert button: add an item
- Delete button: delete an item
- Drag & Drop: Change the order of items
- Shortcut keys: add, delete, change order, copy, paste
- In the case of pasting, it is inserted under the selected module.
- Hex/Bin values are linked and automatically reflected when changed.

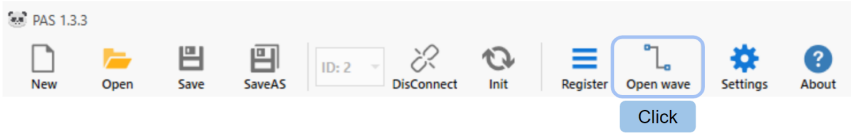
Operations

- Set / GetParameter button: executes the operation of reading or writing the entire register value to the actual device according to the Set/Get feature operation of NAND.
- Users can save or load as a csv file through the file menu.

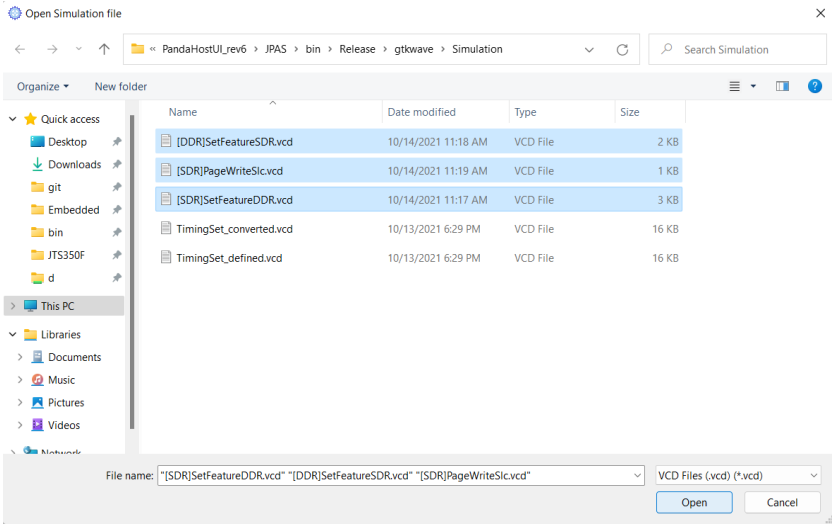
4.9. Debugging with Pattern Simulator

The Wave tool shows a simulated waveform of how the test pattern is actually created.

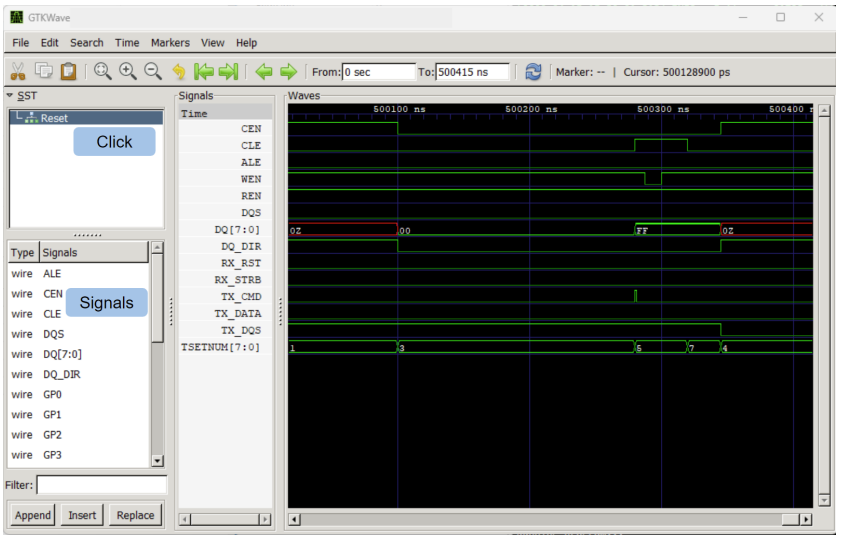
1) Select Settings -> Execution Options -> Create Simulation File option.
2) This option saves the pattern simulation waveform as a .vcd file during the test operation.
3) Clock 'Open Wave' button: The files are downloaded to the Workspace_ID/Simulator path.



4) When the download is complete, a file selection window opens automatically.



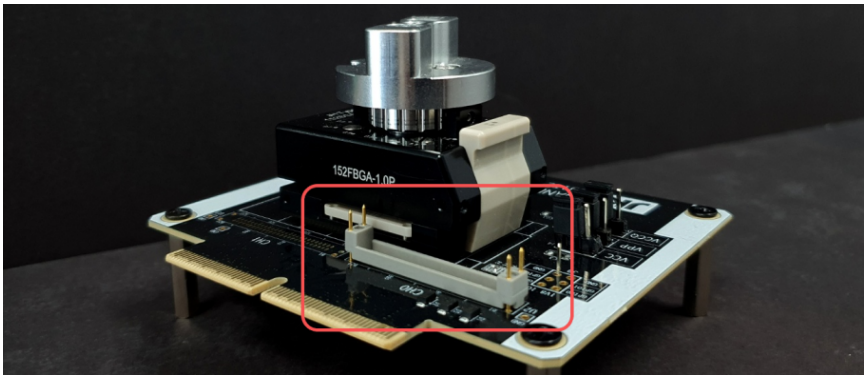
5) If you select the files and press Open, the GTKWave automatically opens the files.
6) You can select and view the desired signal in GTKWave.



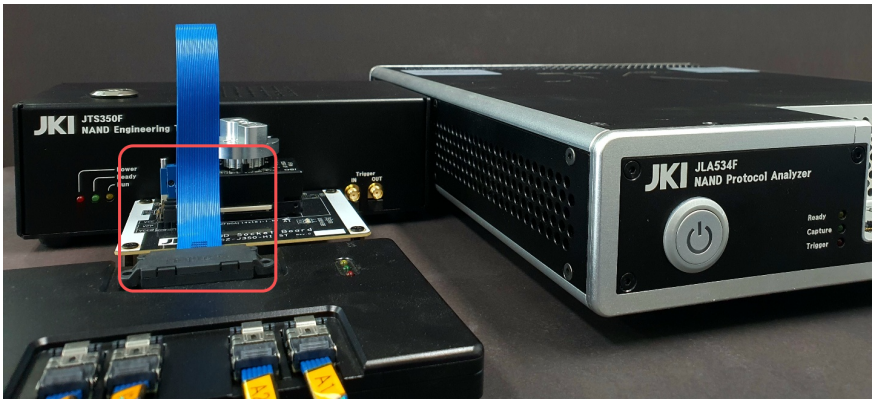
4.10. Debugging with Logic Analyzer

If you want to debug in conjunction with JKI's logic analyzer (JLA434F/JLA534F), you can connect the instrument as follows.

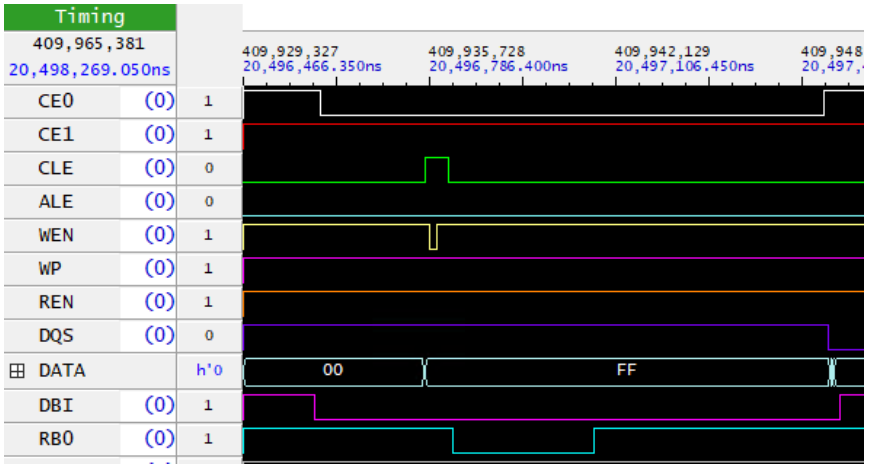
1) Install the Soft Touch Retention module on the socket board.



2) Connect the Soft Touch compatible probe cable to the retention module.



3) While running the test program, check the desired waveform in the JKI logic analysis program.



4.11. File Management

Saving & Opening Tester Settings

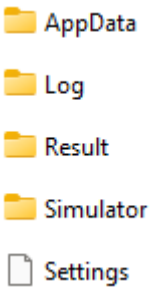
- The Settings file is automatically saved in the workspace with the name “Settings”.
- When the ID is changed, the settings are automatically loaded from that workspace. If the configuration file does not exist, a new configuration file is automatically created.
- When the program ends, the last screen settings and ID are automatically saved.

Saving & Opening Sequence File

- Users can create, save or load sequence files using the buttons below.

Workspace for Multi-Site Testing

- When using multiple testers, the PAS software automatically creates a workspace by the ID in the executable path and organize the test data as follows:



AppData : Temporary file folder created during testing.
Log : A log file during testing. (Saved separately by day)
Result : The result file folder created by the test module
Simulator : Pattern simulator file folder.
Settings : Tester setting file folder for each workspace.

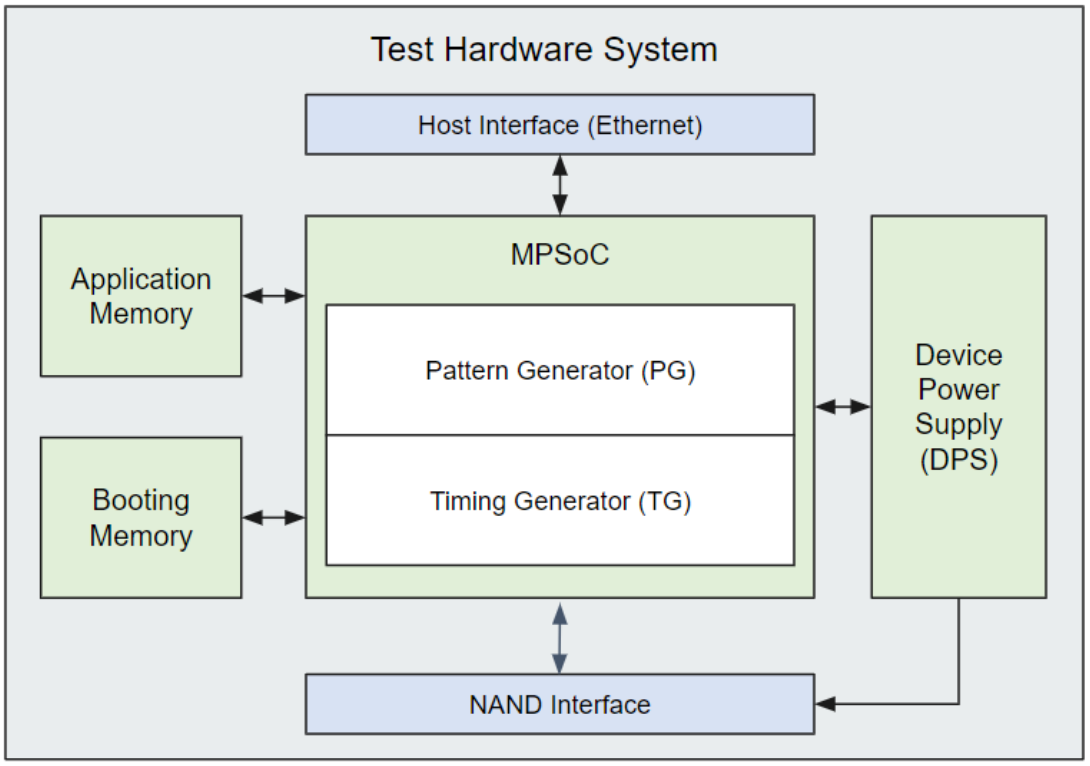
4.12. Keyboard Shortcuts

Key	Description
Ctrl + c	Copy an items
Ctrl + v	Paste an items
Ctrl + d / Ctrl + delete	Delete an items
Ctrl + ↑	Move up an items
Ctrl + ↓	Move down an items
Ctrl + mouse wheel up	Increase the log font size
Ctrl + mouse wheel down	Decrease the log font size

5. Product Specifications

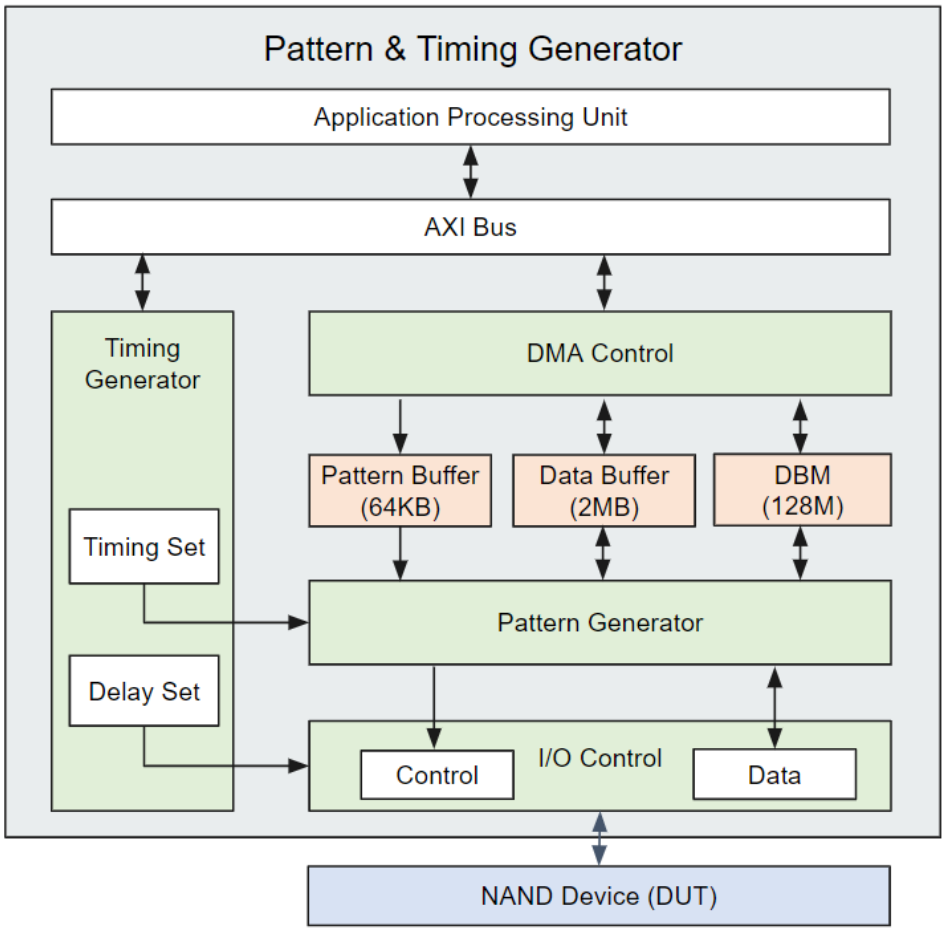
5.1. Test Hardware System

Hardware System Specifications		
Processor	Application Processor	Dual-core ARM Cortex-A53
	Real-time Processor	Dual-core ARM Cortex-R5
Memory	Application Memory	8GB (DDR4)
	Booting Memory	16GB (eMMC)
Host Interfaces	Ethernet	1G Ethernet
	USB	USB 2.0(Client), 3.0(OTG)
Debug Ports	UART	USB to UART Bridge
	JTAG	14 pin / 2.0 mm pitch
NAND Interfaces	HSIO	29 pin * 2 CH
	GPIO	8 pin
Device Power Supply	DPS for NAND	4 channels
	DPS for ETC	4 channels
Pattern & Timing Generator	PG	1 ea
	TG	1 ea



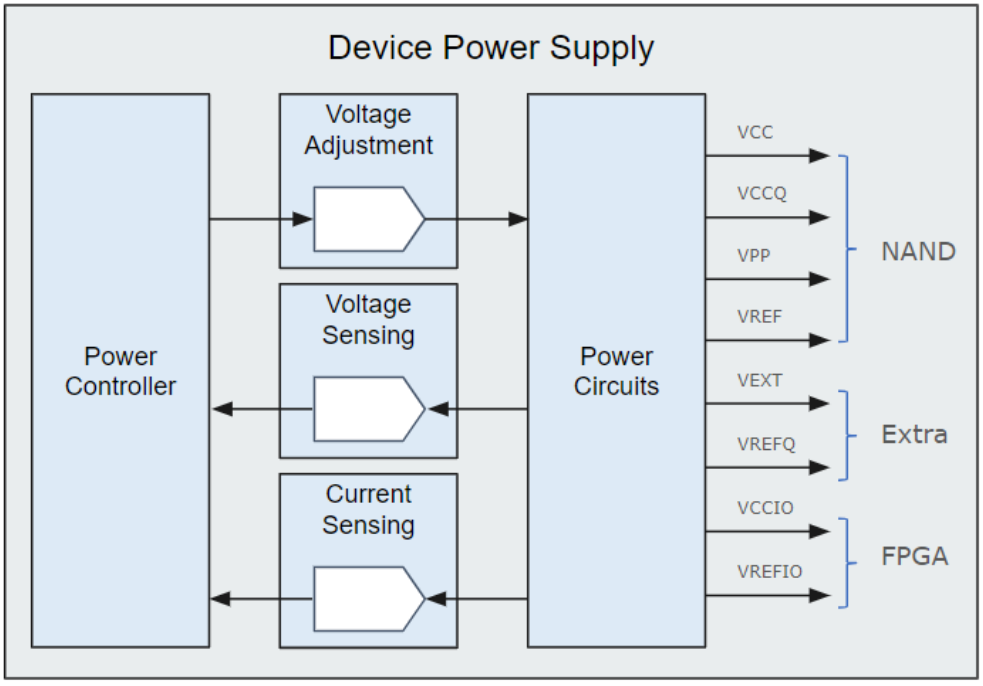
5.2. Pattern & Timing Generator

Pattern & Timing Generator Specifications		
Pattern Memory	Data Buffer Memory (DBM)	64MB(Write), 64MB(Read)
	Read/Write Data Buffer (FIFO)	2MB
	Pattern Buffer (FIFO)	64KB
Timing Generator	Clock Speed (SDR mode)	10 ~ 100 MHz
	Clock Speed (DDR mode)	100 MHz ~ 1200 MHz
	Clock Resolution	1 MHz
	Timing Sets	64 ea
	Number of Edges for each Timing Set	64 ea
	Edge Control Range	1 ~ 256 UI
	Edge Control Resolution	1 UI (0.4 ~ 1.0 ns)
	Delay Control Range	0 ~ 1.5 ns
	Delay Control Resolution	3 ~ 4 ps
NAND Interface Pins	Output (CEn[7:0], Controls)	14 pins * 2-ch
	Input (RBn[3:0])	4 pins * 2-ch
	I/O (DQS, DQ[7:0], DBI)	11 pins * 2-ch
	GPIO	8 pins



5.3. Device Power Supply

Device Power Supply Specifications				
Power Sources	**Setting Range**	**Resolution**	**DC Accuracy**	**Max. Current**
VCC (NAND)	0.8 to 4.0V	<1mV	+/- (1% + 2mV)	3A
VCCQ (NAND)	0.8 to 2.0V	<1mV	+/- (1% + 2mV)	400mA
VPP (NAND)	5.0 to 24V	<1mV	+/- (1% + 20mV)	80mA
VREF (NAND)	0.2 to 4.0V	<1mV	+/- (1% + 2mV)	10mA
VCCIO (FPGA)	0.8 to 2.0V	<1mV	+/- (1% + 2mV)	400mA
VREFIO (FPGA)	0.2 to 2.0V	<1mV	+/- (1% + 2mV)	10mA
VREFQ (Extra)	0.2 to 5.0V	<1mV	+/- (1% + 2mV)	15mA
VEXT (Extra)	1.2 to 30V	<1mV	+/- (1% + 20mV)	10mA



5.4. Environment Conditions

Environment Conditions	
Operating Temperature	0 ~ 55 ℃
Humidity	20% ~ 60 Rh%
Dimensions & Weight	JTS350F: 175 mm x 202 mm x 66 mm (W x L x H), 600 g JTS351F: 190 mm x 109 mm x 66 mm (W x L x H), 600 g
Power Supply	DC 12V / 2A

5.5. NAND Interface Pinout

Pin Name	Attribute	Description
Detect	Input	Connector insert detection (low active)
GND	Ground	Ground
PS_VCC	Power	VCC is NAND device core power supply.
PS_VCCQ	Power	VCCQ is NAND I/O power supply.
PS_VPP	Power	VPP is NAND external high voltage.
PS_VREF	Power	VREF is NAND I/O reference voltage.
PS_VCCIO	Power	VCCIO is FPGA I/O power supply.
PS_5V	Power	5V is spare power supply for reserved use only.
GPIO_1P8[0~3]	GPIO	1.8V general purpose I/O
GPIO_3P3[0~3]	GPIO	3.3V general purpose I/O
CH[0~1]_CEN[0~7]	NAND Input	Chip Enable
CH[0~1]_RNB[0~3]	NAND output	Ready/Busy Output
CH[0~1]_CLE	NAND Input	Command Latch Enable
CH[0~1]_ALE	NAND Input	Address Latch Enable
CH[0~1]_WEN	NAND Input	Write Enable
CH[0~1]_WPN	NAND Input	Write Protect
CH[0~1]_REN+ CH[0~1]_REN-	NAND Input	REN+(RE_t): Read Enable (True) REN-(RE_c): Read Enable Complement
CH[0~1]_DQ[0~7]	NAND I/O	Data Inputs/Outputs
CH[0~1]_DBI	NAND I/O	Data Bus Inversion
CH[0~1]_DQS+ CH[0~1]_DQS-	NAND I/O	DQS+(DQS_t): Data Strobe (True) DQS-(DQS_c): Data Strobe Complement
RESERVED	Reserved	Not used

No	Pin Name	No	Pin Name	No	Pin Name	No	Pin Name
1	Detect	31	GND	61	CH0_REN-	91	CH1_DQ4
3	PS_VCCQ	33	CH0_DQ3	63	GND	93	GND
5	PS_VCCIO	35	GND	65	GND	95	CH1_DQ3
7	PS_VREF	37	CH0_DQ4	67	CH1_REN-	97	GND
9	RESERVED	39	GND	69	CH1_REN+	99	CH1_DQ2
11	GPIO_1P8_0	41	CH0_DQ5	71	GND	101	GND
13	GPIO_1P8_1	43	GND	73	CH1_DQS-	103	CH1_DQ1
15	GPIO_1P8_2	45	CH0_DQ6	75	CH1_DQS+	105	GND
17	GPIO_1P8_3	47	GND	77	GND	107	CH1_DQ0
19	GND	49	CH0_DQ7	79	CH1_DQ7	109	GND
21	CH0_DQ0	51	GND	81	GND	111	GPIO_3P3_0
23	GND	53	CH0_DQS+	83	CH1_DQ6	113	GPIO_3P3_1
25	CH0_DQ1	55	CH0_DQS-	85	GND	115	GPIO_3P3_2
27	GND	57	GND	87	CH1_DQ5	117	GPIO_3P3_3
29	CH0_DQ2	59	CH0_REN+	89	GND	119	Detect

No	Pin Name	No	Pin Name	No	Pin Name	No	Pin Name
2	GND	32	GND	62	CH0_WPN	92	CH1_RNB2
4	PS_5V	34	CH0_RNB0	64	GND	94	CH1_RNB1
6	PS_VPP	36	CH0_RNB1	66	GND	96	CH1_RNB0
8	PS_VCC	38	CH0_RNB2	68	CH1_WPN	98	GND
10	PS_VCC	40	CH0_RNB3	70	CH1_WEN	100	CH1_CEN7
12	GND	42	GND	72	GND	102	CH1_CEN6
14	CH0_CEN0	44	RESERVED	74	CH1_ALE	104	CH1_CEN5
16	CH0_CEN1	46	RESERVED	76	CH1_CLE	106	CH1_CEN4
18	CH0_CEN2	48	GND	78	GND	108	GND
20	CH0_CEN3	50	CH0_DBI	80	CH1_DBI	110	CH1_CEN3
22	GND	52	GND	82	RESERVED	112	CH1_CEN2
24	CH0_CEN4	54	CH0_CLE	86	RESERVED	114	CH1_CEN1
26	CH0_CEN5	56	CH0_ALE	88	GND	116	CH1_CEN0
28	CH0_CEN6	58	GND	90	CH1_RNB3	118	GND
30	CH0_CEN7	60	CH0_WEN	120	RESERVED		

6. Safety and Warranty

6.1. Safety Summary

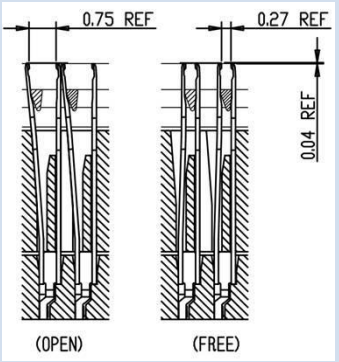
Caution: Before operating your JKI product for the first time, please carefully review the safety guidelines below to avoid any injury and damage.

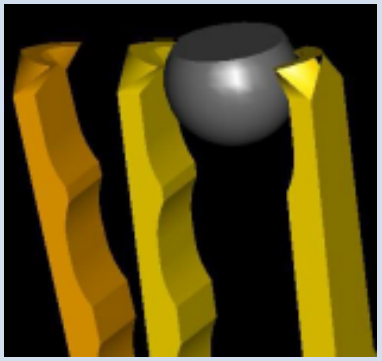
Precaution (ESD)

Since all components of the test board and socket board are exposed to finger touch, special attention should be paid to electrostatic discharge (ESD) precautions. Always get into the habit of first touching the metal surface of one of the USB or Ethernet connectors with both hands for a few seconds before touching any other part of the board. That way you have the same potential as the board, minimizing your ESD risk.

Precaution (EOS)

Do not connect the DUT board while the main board is powered on. Be sure to connect the DUT board while the power is off. Also, when replacing a device in the socket, it must be done with the power off. The pin structure of certain sockets may cause damage to the equipment.





6.2. Warranty and Service

This NAND Tester is provided with a full one year warranty, parts and labor.
Contact your JKI Inc. representative for details.

JKI Inc.

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